SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, Tirupati - 517102

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Three Days FDP on

"Xilinx Zynq-7000 SoC ZC702 Evaluation Kit and Xilinx Vivado Tool"

(06th – 08th December, 2021)

Event Objectives:

1. To impart knowledge in FPGAs and their Applications.
2. To develop skills in modeling algorithms using Xilinx Vivado Tool, analyzing the results and implementing applications using FPGAs.
3. To inculcate attitude towards solving complex engineering problems in the development of FPGA based Designs for various applications.

COURSE OUTCOMES:

After successful completion of the Event, the participants will be able to:

CO1. Apply fundamental knowledge in

- Understanding the functionality of FPGAs.
- Identify the Limiting factors of software implementation of Applications using FPGAs.
- Creating new designs using FPGAs to solve problems of implementation of algorithms related to image processing.

CO2. Analyze the functioning of FPGAs and their applications.

CO3. Design solutions for complex implementations for applications using Zynq – 7000

FPGAs.

CO4. Use Xilinx Vivado Tools to develop the applications of FPGAs for image processing and assess the performance of the design.

CO - PO Mapping:

	PO1	PO2	PO3	PO5
CO1	√			
CO2		√		√
CO3			√	
CO4				√

Event Description:

The FPGAs gained popularity recently due to their flexibility and adaptability to new designs. The purchased Zynq – 7000 series ZC702 FPGA has the following features - Optimized for quickly prototyping embedded applications using Zynq-7000 SoCs, Hardware, design tools, IP, and pre-verified reference designs, Demonstrates an embedded design, targeting video pipeline, Advanced memory interface with 1GB DDR3 Component Memory, Enabling serial connectivity with USB OTG, UART, IIC, and CAN Bus, Supports embedded processing with Dual ARM Cortex-A9 core processors, Develop networking applications with 10-100-1000 Mbps Ethernet (GMII, RGMII, and SGMII), Implement video display applications with HDMI out and Expand I/O with the FPGA Mezzanine Card (FMC) interface. These features enable us to use for image processing applications for telemedicine especially as the project requires for Fundus image processing to aid patients and doctors to take the right decision even if the images get distorted during wireless transmission.

Training was provided by Mr. K. Pradeep on 06th December 2021 and followed by Ms. Neelima K on 07th and 08th December 2021, on

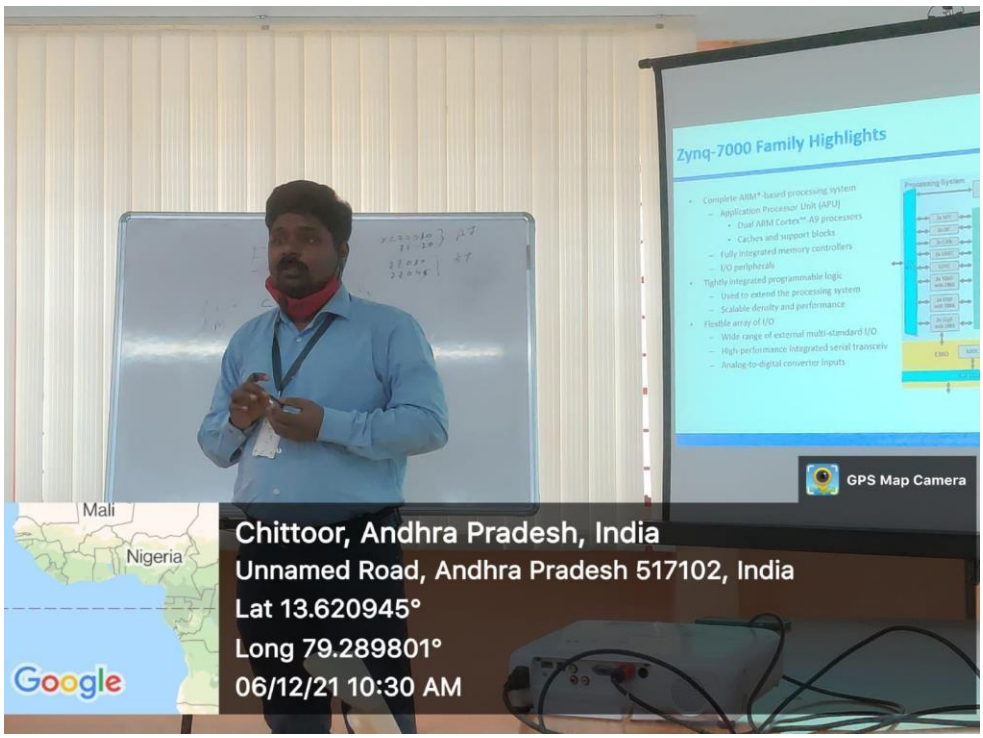
- ✓ Introduction to FPGAs.
- ✓ Zynq – 7000 SoC ZC702 Evaluation Kit complete pin description and functionality of each block.
- ✓ Xilinx System Generator based Image Processing – Image Enhancement is developed. The image results were analyzed and the Zynq – 7000 SoC ZC702 FPGA was interfaced to obtain the processed image.
- ✓ The Xilinx Vivado Tool basic design flow for HDL based entry along with synthesis and implementation results were analyzed by interfacing Zynq – 7000 series FPGA.

Total Number of Faculty Registered : 10

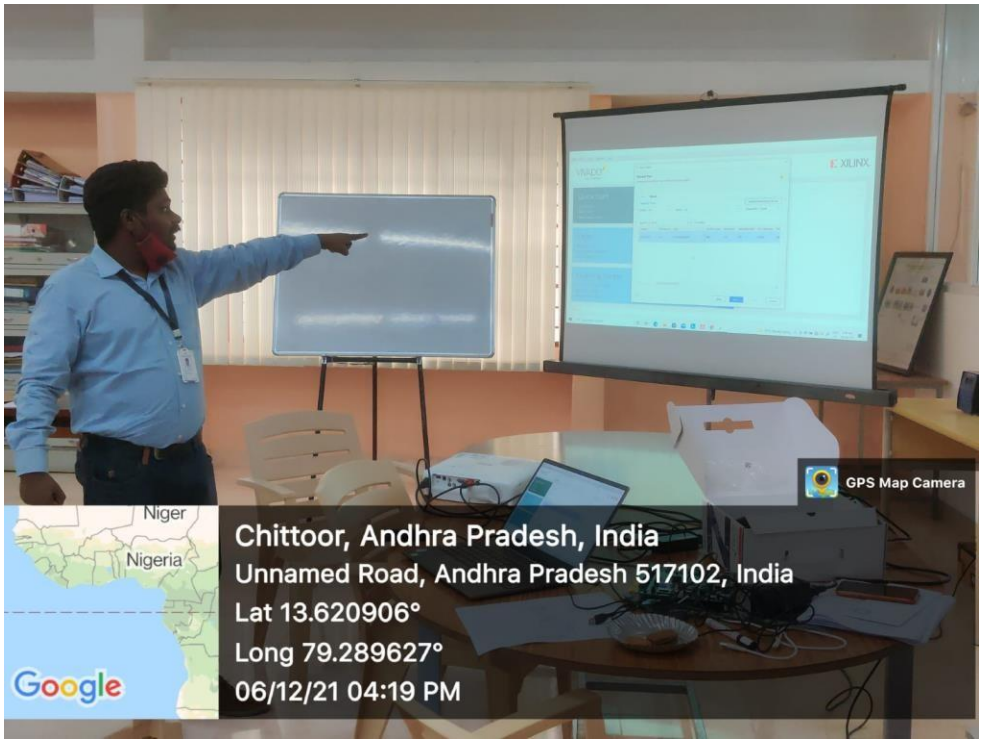
Total Number of Faculty Attended : 10

Geotagged Photos:

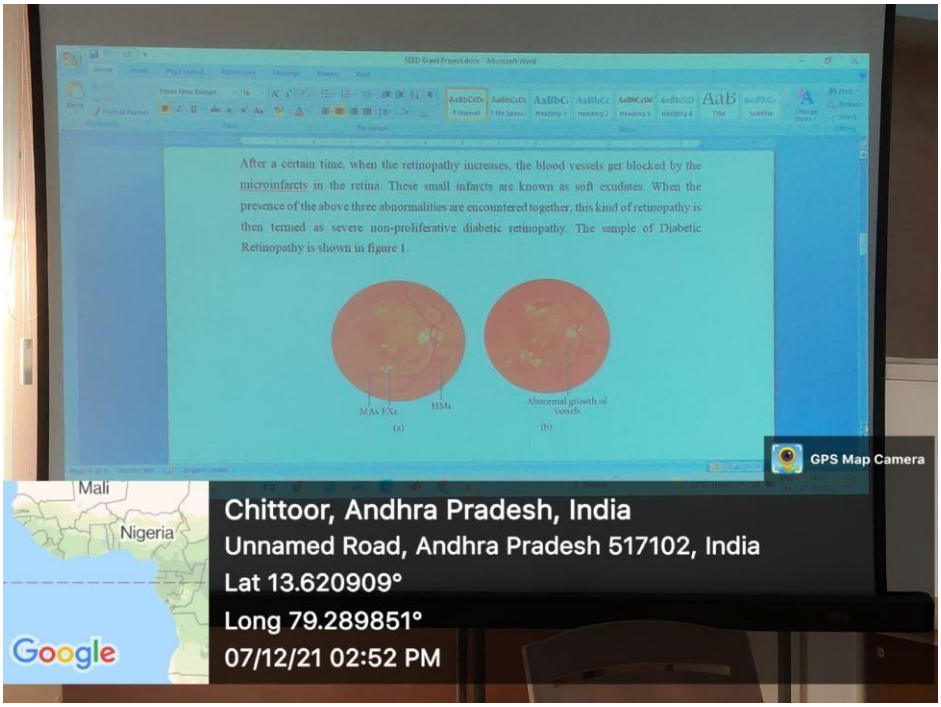
The above figure shows the FPGA Purchased – Zynq 7000 series ZC702.



The above figure shows the resource person explaining about the purchased FPGA features and functionality.



The above figure shows the Xilinx Vivado Design Flow in software being explained by the resource person.



The above figure shows the fundus images as required by seed grant proposal as explained by Ms. Neelima K to the attendees.

The above figure shows the evaluation of image processing algorithm theoretically as proposed and explained by Ms. Neelima K to the attendees.

The above figure shows the description of FPGA purchased with various available for practical usage being explained by Ms. Neelima K to the attendees.

The above figure shows the software evaluation of designed algorithm being explained by Ms. Neelima K to the attendees.