MINOR DEGREES OFFERED UNDER SVEC-19 REGULATIONS

Offering Dept.	Title of the Minor	Students of Eligible Branches
CSE	Artificial Intelligence and Machine Learning	All branches except CSE, IT and CSSE
IT	Internet of Things	All branches except IT
CSSE	Cyber Security	All branches except CSE, IT and CSSE
ECE	VLSI and Embedded Systems	All branches except ECE
EEE	Power Systems and Drives	All branches except EEE
EIE	Instrumentation and Control Engineering	All branches except EIE
ME	Robotics	All branches except ME
CE	Sustainable Engineering	All branches except CE

Academic Regulations for Minor Degree:

The concept of Minor degree is introduced in the curriculum of all B.Tech. programs offering a Major degree. The main objective of Minor degree in a discipline is to provide additional learning opportunities for academically motivated students and it is an optional feature of the B.Tech. Program. To earn a Minor degree in a discipline, a student has to earn 18 extra credits (By studying FIVE theory & THREE laboratory courses or SIX Theory Courses) from the core courses of the minor discipline.

a. Students having a CGPA of 8.0 or above up to II B.Tech I-Semester without any backlogs shall be permitted to register for a Minor degree by paying the requisite fee.

b. In the subsequent semesters, the student has to pass all the courses registered for Major and Minor Degrees in the first attempt i.e., regular examinations without any backlog to keep the Minor Degree registration active or else it shall be cancelled.

c. If a student becomes ineligible for continuing the Minor Degree, the earned credits under Minor Degree cannot be transferred to Major

Degree; they will remain extra. These additional courses will be mentioned in the transcript. However, they are eligible to receive B.Tech. Degree after satisfying its requirements.

d. The evaluation pattern of the courses shall be similar to the evaluation of regular program courses.

e. Minimum strength required for offering Minor Degree in a discipline is 40 students.

f. A student registered for Minor degree shall pass in all subjects that constitute the requirement for the Minor degree program. No class/division (i.e., second class, first class and distinction, etc.) shall be awarded for Minor degree program.

g. The Minor degree shall be mentioned in the degree certificate as Bachelor of Technology in XXX with Minor in YYY. For example, Bachelor of Technology in Computer Science & Engineering with Minor in Title of the Minor Pursued. This shall also be mentioned in the transcripts, along with the list of courses taken for Minor degree program. However, the performance of the student in the Minor courses will not be considered for the calculation of SGPA and CGPA for the award of Major Degree.

h. Separate course/class work and time table shall be arranged for the various Minor degree programs. Attendance regulations for these Minor discipline programs shall be as per regular courses.

i. Students aspiring for Minor degree must register from III B.Tech I-Semester onwards and must opt for a Minor in a discipline other than the discipline he is registered in.

j. A Student shall register for Minor with the following combinations:

Offering Theory and Laboratory Courses: SEVEN credits in a semester starting from III B.Tech I-Semester to III B.Tech II-Semester (TWO theory & ONE laboratory courses) and FOUR credits in IV B.Tech I-Semester (ONE theory & ONE laboratory courses).

Offering Theory Courses only: SIX credits in a semester starting from III B.Tech I-Semester to IV B.Tech I-Semester (TWO theory courses).

NOTE: Interested meritorious students shall be permitted to register either for a Minor degree in a discipline (or) Honors Degree in a discipline only, but not both.

MINOR DEGREE IN

VLSI AND EMBEDDED SYSTEMS

Offering Department: ELECTRONICS AND COMMUNICATION ENGINEERING

Students of Eligible Branches: CSE, CSSE, IT, EEE, EIE, ME and CE

COURSE STRUCTURE

Year &Semester	Course code	Course title	Contact Periods per week			C	Scheme of Examination Max. Marks		
			L	T	P		Int. Marks	Ext. Marks	Total Marks
III B.Tech. I-Sem (2 Theory+ 1 Lab)	19BM50401	Switching Theory and Logic Design	3	-	-	3	40	60	100
	19BM50402	VLSI Design	3	-	-	3	40	60	100
	19BM50403	Microcontrollers	3	-	-	3	40	60	100
	19BM50431	Digital design Lab	-	-	2	1	40	60	100
III B.Tech. II-Sem. (2 Theory+ 1 Lab)	19BM60401	ARM and AVR Microcontrollers	3	-	-	3	40	60	100
	19BM60402	Testing and Testability	3	-	-	3	40	60	100
	19BM60403	Low Power CMOS VLSI Design	3	-	-	3	40	60	100
	19BM60404	Microprocessors and Microcontrollers	3	-	-	3	40	60	100
	19BM60431	VLSI Lab	-	-	2	1	40	60	100
IV B.Tech. I-Sem. (1 Theory+ 1 Lab)	19BM70401	Embedded Systems	3	-	-	3	40	60	100
	19BM70402	Real Time Systems	3	-	-	3	40	60	100
	19BM70403	System-on-Chip Design and verification	3	-	-	3	40	60	100
	19BM70431	Embedded Systems Lab	-	-	2	1	40	60	100

Note: If any student has chosen a course from the above list in their regular curriculum then, he/she is not eligible to opt the same course/s for the Minor degree. It is the responsibility of the student to acquire/complete prerequisite before taking the respective course.

III B. Tech. – I Semester
(19BM50401) SWITCHING THEORY AND LOGIC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: -

COURSE DESCRIPTION: Number system and Boolean algebra; Minimization; Analysis and synthesis of digital circuits; Asynchronous Sequential Logic & Programmable Memories.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Demonstrate the knowledge of Boolean Algebra, various number systems and Logic gates to implement Digital Circuits.

CO2: Design subsystem by Analyzing combinational & sequential logic circuits for providing optimal solutions

CO3: Develop Asynchronous sequential logic and programmable memories for societal needs.

CO4: Design various programmable logic arrays using logic gates

DETAILED SYLLABUS:

UNIT-I: NUMBER SYSTEMS AND BOOLEAN ALGEBRA (10 Periods)

Digital systems, Binary Numbers, Number base conversions, Complements of numbers, Signed binary numbers, Binary codes, Error detection and correction codes. Boolean Algebra-Basic definition, Basic theorems and properties, Boolean Functions, Canonical & Standard forms, logic operations & Logic gates.

UNIT-II: GATE LEVEL MINIMIZATION (08 Periods)

The map method, four variable, Five variable K-map, POS & SOP Simplification, Don't care conditions, NAND & NOR Implementation, Other two level Implementation, Ex-or Function, Tabular Method- Simplification of Boolean function using tabulation Method.

UNIT-III: COMBINATIONAL LOGIC DESIGN (09 Periods)

Combinational circuits, Analysis & Design procedure, Binary Adder-Sub tractor, Decimal Adder, Binary Multiplier, Magnitude comparator, Decoder, Encoders, Multiplexers and De- Multiplexers.

UNIT-IV: SEQUENTIAL LOGIC DESIGN (11 Periods)

Sequential Circuits, Latches, Flip-Flops, Analysis of Clocked sequential circuits, State Reduction & Assignment, Design procedure, Introduction to Registers-Universal Shift Registers, Introduction to Counters, Ripple Counters-Binary and BCD Ripple Counter , Synchronous counters-Binary, Up-Down Binary Counter and BCD Counter and Other counters-Ring Counter, Johnson Counter.

UNIT-V: ASYNCHRONOUS SEQUENTIAL LOGIC AND PROGRAMMABLE MEMORIES (07 Periods)

Introduction, Analysis procedure, Design Procedure-Primitive Flow Table, Reduction of State and Flow Tables-Implication Table and Implied States, Hazards, ROM, PLA, PAL.

Total Periods: 45

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOK:

1. M. Morris Mano, Michael D. Ciletti, *Digital Design With an Introduction to the Verilog HDL*, Pearson, 5th edition, 2017.

REFERENCE BOOKS:

1. A. Anand Kumar, *Switching Theory and Logic Design*, PHI Learning Private Limited, 3rd edition, India, 2017.
2. Charles H. Roth, Jr. and Larry L. Kinney, *Fundamentals of Logic Design*, Cengage Learning, 7th edition, 2015

CO-PO-PSO Mapping Table

Course outcome	Program Outcomes														
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
CO1	3	-	-	-	-	-	-	**-**	**-**	**-**	**-**	**-**	3	**-**	**-**
CO2	3	2	3	1	-	1	1	**-**	**-**	**-**	**-**	**-**	3	**-**	**-**
CO3	3	2	3	1	-	1	1	**-**	**-**	**-**	**-**	**-**	3	**-**	**-**
CO4	3	2	3	1	-	1	1	**-**	**-**	**-**	**-**	**-**	3	**-**	**-**
Average	3	2	3	1	-	1	1	**-**	**-**	**-**	**-**	**-**	3	**-**	**-**
Course Correlation Level	**3**	**2**	**3**	**1**	**-**	**1**	**1**	**-**	**-**	**-**	**-**	**-**	**3**	**-**	**-**

Correlation Level: 3-High ; 2-Medium ; 1-Low

III B. Tech. – I Semester

(19BM50402) **VLSI Design**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: A Course on Switching Theory and Logic Design/Digital Logic Design.

COURSE DESCRIPTION: Logic Families; CMOS Technology; Stick Diagrams and Layouts; Subsystem design; Programmable Interconnect structures; Memories.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze logic families, steady state and dynamic characteristics of CMOS, to improve performance characteristics of digital ICs.
CO2: Analyze electrical properties of MOS circuits for VLSI/ULSI chip fabrication.
CO3: Develop stick diagrams and layouts of CMOS circuits for miniaturization by analyzing gate delays and scaling effects.
CO4: Design subsystems for High speed digital electronics to compensate tradeoff among area, speed and power requirements.

DETAILED SYLLABUS:

UNIT-I: DIGITAL LOGIC FAMILIES (08 Periods)

Introduction to logic families, RTL, DTL, Transistor-Transistor logic, Emitter Coupled Logic, I^2L, CMOS logic, CMOS steady state and dynamic electrical behavior.

UNIT-II: FABRICATION AND ELECTRICAL PROPERTIES OF MOS (10 Periods)

Fabrication Process for NMOS and CMOS technology, Basic Electrical Properties of MOS: I_{ds} – V_{ds} relationships, Second order effects of MOSFETs-Latch up, Hot carrier Effects, channel length modulation, Threshold Voltage V_T, g_m, g_{ds} and ω_0; Pass Transistor, NMOS inverter, Pull up to pull down ratio for an NMOS inverter, CMOS Inverter

UNIT-III: CMOS CIRCUIT DESIGN PROCESS (10 Periods)

VLSI design flow, MOS layers, stick diagrams, NMOS design style, CMOS design style, lambda based design rules, layouts for inverters, sheet resistance, capacitances of layers, Gate delays, Delay estimation, Scaling, Limitations of Scaling.

UNIT-IV: SUBSYSTEM DESIGN - I (08 Periods)

Adders – Transmission based Adder, Carry look-ahead adder, Manchester carry chain adder, Carry Skip Adder, Carry Select Adder; Barrel Shifter, Multipliers – Array Multiplier, Booth Multiplier; ALUs.

UNIT-V: SUBSYSTEM DESIGN - II **(09 Periods)**

Counters- Synchronous and Asynchronous Counter; High Density Memory Elements - Design Approach, FPGAs, Programmable Interconnect structures - Fusible links, Antifuse via link, UV Erasable, Electrically Erasable; CPLDs, Cell based Design Methodology.

Total Periods: 45

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOKS:

1. Kamran Eshraghian, Douglas A. Pucknell and sholeh Eshraghian, *Essentials of VLSI Circuits and Systems*, PHI, 2005.
2. Morris Mano, *Digital Design*, Prentice Hall, 3rd Edition, 2003 .

REFERENCE BOOKS:

1. John F.Wakerly, *Digital Design Principles & Practices*, Pearson Education Asia, 4th Edition, 2008.
2. John M. Rabaey, *Digital Integrated Circuits: A Design Perspective*, PHI, 2nd Edition, 2003.

CO-PO-PSO Mapping Table

Course outcome	Program outcomes														
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO3	3	2	3	2	-	-	-	2	-	-	-	-	3	-	-
CO4	3	2	3	2	-	1	1	2	-	-	-	-	3	-	-
Average	3	2.5	3	2	-	1	1	2	-	-	-	-	3	-	-
Course Correlation Level	**3**	**3**	**3**	**2**	**-**	**1**	**1**	**2**	**-**	**-**	**-**	**-**	**3**	**-**	**-**

Correlation Level: 3-High ; 2-Medium ; 1-Low

III B. Tech. - I semester

(19BM50403) **MICROCONTROLLERS**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: A Course on Switching Theory and Logic Design/Digital Logic Design.

COURSE DESCRIPTION: 8051 Microcontroller - Architecture, programming, interrupts and applications; PIC microcontroller architecture, Interrupts and timers of PIC microcontroller, interfacing

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze Architectural features and Instruction Set of 8051 for control applications.

CO2: Analyze PIC18 Architecture and Instruction Set to develop computing applications.

CO3: DevelopPrograms for PIC18 using ports, timers and associated on Chip resources for Specified Applications.

CO4: Design microcomputer based systems with the knowledge of Interfaces and Peripherals of PIC18 to Solve various engineering problems.

DETAILED SYLLABUS:

UNIT-I: 80C51/31 (10 Periods)

Microprocessors vs Microcontrollers, 8051 Architecture, Internal and external memories, Addressing modes, Timers/Counters structure & configuration, Instruction set of 8051, simple programs using 8051.

UNIT-II: PIC ARCHITECTURE & PROGRAMMING (10 Periods)

Architecture of PIC18, Register Organization, Memory Organization - ROM space & RAM; Data formats & Directives, Instruction Set: Arithmetic, Logic, branching, Bit wise, bank switching, Simple PIC Programs.

UNIT-III: PORTS, TIMERS & PROGRAMMING (10 Periods)

Pin description of PIC18F452, Basic Port Structure, I/O port programming; Macros and modules, Structure of Timer 0 & its Programming using Assembly and C, Counter programming, Structure of timers 1, 2 and 3 & their Programming.

UNIT-IV: PIC - SERIAL PORT AND INTERRUPTS (07 Periods)

Basics of communication – Serial/Parallel, RS232 & PIC18 connection to RS232, Serial Port Structure & programming; PIC18 interrupts, Programming timer interrupts, Programming serial interrupts.

UNIT-V: PIC INTERFACING (08 Periods)

7 segment LED and LCD interfacing, keyboard interfacing, interfacing ADC, DAC, Interfacing DC motor, stepper motor, PWM using CCP.

Total Periods: 45

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOKS:

1. Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D, *The 8051 Microcontroller and Embedded Systems-using assembly and C,* PHI, 2006/ Pearson New International Edition 2014
2. Muhammad Ali Mazidi, Rolin D. McKinlay, Danny causey, *PIC Microcontroller and Embedded Systems: Using C and PIC18*, Pearson Education, 2015.

REFERENCE BOOKS:

1. Kenneth J. Ayala, *The 8051 Microcontroller-Architecture, Programming & Applications,* 3rd Edition, Cengage learning, June 2007.
2. Ramesh S. Gaonkar, *Fundamentals of Microcontrollers and Applications in Embedded Systems (With PIC18 Microcontroller Family),* Penram International, 2010.
3. M Rafiquzzaman, *Microcontroller Theory And Applications With The PIC,* Wiley India Publications, March 2014

ADDITIONAL LEARNING RESOURCES:

1. http://crystal.uta.edu/~zaruba/CSE3442/
2. https://owd.tcnj.edu/~hernande/ELC343/
3. http://www.ciebookstore.com/Content/Images/uploaded/PIC18-Study-Guide-CIE.pdf

CO-PO-PSO Mapping Table

Course outcome	Program outcomes														
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO2	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO3	3	2	3	-	-	1	-	-	-	-	-	-	3	-	-
CO4	3	2	3	1	-	1	-	1	-	-	-	-	3	-	-
Average	3	2.5	3	1	-	1	-	1	-	-	-	-	3	-	-
Course Correlation Level	3	3	3	1		1		1	-	-	-	-	3	-	-

Correlation Level: 3-High ; 2-Medium ; 1-Low

III B. Tech. – I Semester

(19BM50431) **DIGITAL DESIGN LAB**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	-	-	2	1

PRE-REQUISITES: Courses on Switching Theory and Logic Design/Digital Logic Design & Electronic Devices and Circuits.

COURSE DESCRIPTION: Design and verification of Digital Circuits, PCB Design of Electronic Circuits.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Design and Realize various Digital applications by using ICs for societal needs.
CO2: Implement Electronic Circuits using Passive and Active elements for specified applications.
CO3: Analyze performance parameters for PCB designed circuits using a simulation tool.
CO4: Work independently and in teams to solve problems with effective Communication.

LIST OF EXERCISES/LIST OF EXPERIMENTS:

Part-A: Realize the Following in Hardware

(Minimum **Six** Experiments are to be conducted)

1. Realize gates using NAND & NOR gates.
2. Optimize and Realize a given Boolean Function.
3. Design and Realize BCD to Excess-3 Code Converter.
4. Design and Realize Adder and Subtractor using Multiplexer based on logic gates/ IC74153.
5. Design and Realize a BCD to 7-Segment Decoder using Logic Gates/ ICs.
6. Design and Realize a Hexadecimal to Binary Encoder using IC74148 and IC74157.
7. Design and Realize a Sequence Generator using IC7495.
8. Design and Realize Asynchronous and Synchronous counters using IC7476 (JK-Flip Flop).

Part-B: PCB Layout Design of Electronic Circuits using TINAPRO/ eSIM-KiCAD/ TinyCAD/ Fritzing Software

*(Minimum **Four** Experiments are to be conducted)*

1. RC Filter.
2. Half Wave Precision Rectifier.
3. Zener Regulator.
4. Diode Clamper.
5. Transistor as a Switch.
6. CMOS Inverter.

REFERENCE BOOKS/LABORATORY MANUALS:

1. John F. Wakerly, *Digital Design Principles & Practices*, Pearson Education Asia, 4th Edition, 2008.

SOFTWARE/Tools used:

TINAPRO/ eSIM-KiCAD/ TinyCAD PCB Design Tool.

ADDITIONAL LEARNING RESOURCES:

1. http://vlabs.iitb.ac.in/vlabsdev/vlab_bootcamp/bootcamp/cool_developers/index.html - Virtual labs for digital circuits
2. https://nptel.ac.in/courses/108/108/108108031/
3. https://swayam.gov.in/nd2_aic20_sp59/preview

CO-PO-PSO Mapping Table

Course outcome	Program Outcomes														
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
CO1	3	2	3	-	2	2	2	2	-	-	-	-	3	-	-
CO2	3	2	3	-	2	2	2	2	-	-	-	-	3	-	-
CO3	3	3	2	-	3	2	-	-	-	-	-	-	3	-	-
CO4	-	-	-	-	-	-	-	-	3	3	-	-	-	-	-
Average	3	2.33	2.66	-	2.33	2	2	2	3	3	-	-	3	-	-
Course Correlation Level	**3**	**3**	**3**	**-**	**3**	**2**	**2**	**2**	**3**	**3**	**-**	**-**	**3**	**-**	**-**

Correlation Level: 3-High ; 2-Medium ; 1-Low

III B. Tech. – II Semester

(19BM60401) **ARM AND AVR CONTROLLERS**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: Courses on Switching Theory and Logic Design/Digital Logic Design,& Microcontrollers

COURSE DESCRIPTION: ARM Architecture; ARM Instruction Set; ARM Programming; AVR Architecture; AVR Programming in Assembly Language & C

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze ARM Architectures and Instruction Set to develop fundamental Programs.
CO2: Develop efficient ARM based Prototypes by analyzing modes of ARM operation to program ARM Cortex M3 at Assembly and high levels.
CO3: Realize efficient Embedded Systems with an understanding of limitations by evaluating architectural features of AVR Family Microcontrollers .
CO4: Apply Programming techniques at Assembly and High Level to develop industry standard microcontroller based systems.

DETAILED SYLLABUS:

UNIT-I: INTRODUCTION TO ARM ARCHITECTURE (09 Periods)

Introduction to ARM family of processors and controllers, Architecture of ARM Cortex M3, Cortex M3 fundamentals, registers, Operation modes, ARM Instruction Set: Data transfer, Data Processing Call & Branch, Bit Manipulation, Pseudo Instructions and other useful instructions in Cortex M3, ARM Assembly Language Programming.

UNIT-II: THUMB PROGRAMMING & OTHER ARM FEATURES (09 Periods)

Thumb Instruction Set, ARM Mode & Thumb mode Programming, ARM Programming in C. Memory system, memory map, Memory system attributes, ARM Pipeline, Exception types, Cortex M3 Processor applications.

UNIT-III: INTRODUCTION TO AVR MICROCONTROLLER (09 Periods)

Overview of AVR family, AVR Microcontroller architecture, status register, Special function registers, RAM, ROM & EEPROM space, On-Chip peripherals, ATmega32 pin configuration & function of each pin, Fuse bits of AVR.

UNIT-IV: AVR ASSEMBLY LANGUAGE PROGRAMMING (10 Periods)

AVR data types and assembler directives, Addressing modes of AVR, Data transfer, Arithmetic, Logic and Compare, Rotate and Shift, Branch and Call instructions, AVR studio setup for assembly language programming, AVR I/O Port Programming, Time delay loop, Look-up table, Bit addressability, MACROs, Intel HEX file.

UNIT-V: AVR PROGRAMMIN IN C **(08 Periods)**

AVR Data types, AVR I/O port programming, Timer programming, Input capture and Wave Generator, PWM programming External Interrupt programming, ADC programming, EEPROM programming.

Total Periods: 45

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOKS:

1. Joseph Yiu, *The Definitive Guide to the ARM Cortex-M3 & M4*, Elsevier, 3rd Edition, January 2014.
2. Muhammad Ali Mazidi, Sarmad Naimi and SepehrNaimi*, The AVR Microcontroller and Embedded Systems Using Assembly and C*, Pearson Education, January 2014.

REFERENCE BOOKS:

1. Ramesh Gaonkar, *Fundamentals of Microcontrollers and Applications in Embedded Systems (with the PIC18 Microcontroller Family)*, Penram International, First edition,2010
2. Andrew Sloss, Dominic Symes, Chris Wright, *ARM System Developer's Guide: Designing and Optimizing System Software* (The Morgan Kaufmann Series in Computer Architecture and Design), October 2004.
3. AVR ATmega32 data sheet

CO-PO-PSO Mapping Table

Course outcome	Program Outcomes														
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	2	2	-	-	-	-	**-**	**-**	**-**	**-**	2	2	1
CO2	3	3	3	2	2	1	-	-	**-**	**-**	**-**	**-**	2	2	1
CO3	3	3	3	2	1	1	2	3	**-**	**-**	**-**	**-**	2	1	1
CO4	3	2	3	2	3	1	3	2	**-**	**-**	**-**	**-**	-	1	1
Average	3	2.7	2.7	2	2	1	2.5	2.5	-	**-**	**-**	**-**	2	1.5	1
Course Correlation Level	**3**	**3**	**3**	**2**	**2**	**1**	**3**	**3**	**-**	**-**	**-**	**-**	**2**	**2**	**1**

Correlation Level: 3-High ; 2-Medium ; 1-Low

III B. Tech. – II Semester

(19BM60402) **TESTING AND TESTABILITY**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: A Course on VLSI Design.

COURSE DESCRIPTION: Need for Testing, Types of Testing, Fault Modeling, Test Methods for evaluation, Test Generation Algorithms, Delay Tests, IDDQ Tests, Ad-Hoc DFT Methods, Scan Based Designs, Built-In Self Test.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Understand the importance of Testing, fault models and related theorems.
CO2: Analyze various test methods, combinational and sequential circuit test generation Algorithms for Functional Verification of Digital Circuits.
CO3: Analyze delay test algorithms and IDDQ test algorithms for at-speed testing of CMOS Integrated Circuits.
CO4: Understand the concepts and architectures for Built-In Self Testto satisfy industry specifications.

DETAILED SYLLABUS:

UNIT-I: INTRODUCTION TO TESTING (09 Periods)

Role of Testing, VLSI Technology Trends Affecting Testing, Types of Testing, Test Economics, Yield, Fault Modeling, Fault Equivalence, Fault Collapsing, Fault Dominance and Checkpoint Theorem.

UNIT-II:– TEST METHODS (10 Periods)

Simulation for Design Verification and Test Evaluation, Algorithms for Fault Simulation – Serial, Parallel, Deductive, Concurrent Fault Simulations; Fault Sampling.

UNIT-III: COMBINATIONAL AND SEQUENTIAL CIRCUIT TEST GENERATION (11 Periods)

ATPG Algorithms – D-Algorithm, PODEM, FAN; Test Compaction, Time Frame Expansion Method – Nine-Value Algorithm; Simulation Based Sequential ATPG - CONTEST Algorithm.

UNIT-IV: DELAY AND IDDQ TESTS (06 Periods)

Delay Test – Path-Delay Test, Transition Faults, At-Speed Testing; IDDQ Test – Limitations, Delta IDDQ Testing, IDDQ Built-in Current Testing.

UNIT-V: DESIGN FOR TESTABILITY (09 Periods)

Ad-Hoc DFT Methods, Full Scan Design, Partial Scan Design, Random Logic BIST – Test-per-Clock and Test-per-Scan BIST Systems; Boundary Scan Standard – TAP Controller and Port.

Total Periods: *45*

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOK:

1. Michael L. Bushnell, Vishwani D. Agrawal, "*Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits"*, Kluwer Academic Pulishers, Springer US, New York, 2006.

REFERENCE BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, *"Digital Systems Testing and Testable Design",* Wiley, Jaico Publishing House, 1st Edition, 2001.
2. Alfred L. Crouch, "*Design for Test for Digital ICs & Embedded Core Systems*", Pearson Education, 1st Reprint Edition, 2007.
3. Robert J.Feugate, Jr., Steven M.Mclntyre, "*Introduction to VLSI Testing*", Prentice Hall, 1st Illustrated Edition,1998.

ADDITIONAL LEARNING RESOURCES:

1. https://www.classcentral.com/course/swayam-digital-vlsi-testing-7956

CO-PO-PSO Mapping Table

Course outcome	Program outcomes												Program specific outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	-	-	-	-	-	-	-	-	-	-	-	3	-	-
CO2	3	3	2	2	2	-	-	-	-	-	-	-	3	-	-
CO3	3	3	2	2	2	-	2	3	-	-	-	-	3	-	-
CO4	3	-	-	-	-	-	-	3	-	-	-	-	3	-	-
Average	3	3	2	2	-	-	2	3	-	-	-	-	3	-	-
Course correlation Level	**3**	**3**	**2**	**2**	**-**	**-**	**2**	**3**	**-**	**-**	**-**	**-**	**3**	**-**	**-**

Correlation Level: 3-High ; 2-Medium ; 1-Low

III B. Tech. - II semester

(19BM60403) **LOW POWER CMOS VLSI DESIGN**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: A Course on VLSI Design.

COURSE DESCRIPTION: Basic Principles; Methodologies and techniques of CMOS Circuit Designs; Need For Low Power VLSI Design; Principles Of Low Power Circuit Design; Simulation Analysis of Low Power; Logic and Circuit Analysis; Special Techniques and Advanced Techniques Of Low Power Design; Performance Management in Architecture or System level.

COURSE OUTCOMES: After successful completion of this course, the students will be able to

CO1: Demonstrate low power design requirements for CMOS VLSI circuits.
CO2: Analyze and estimate power at Logic and Circuit abstraction levels of digital systems.
CO3: Develop alternate circuits and logic for analysis of low power circuits.
CO4: Apply special and advanced low power techniques at circuit, architecture and systemlevels to develop CMOS devices.

DETAILED SYLLABUS:

UNIT-I: BASICS OF LOW POWER DESIGN (07 Periods)

Needs For Low Power VLSI Chips, Charging And Discharging Capacitances, Short Circuit Current in CMOS, CMOS Leakage Current, Static Current, Basic Principles Of Low Power Design, Low Power Figure Of Merits, Low Power VLSI Design Limits.

UNIT-II: POWER ANALYSIS AND ESTIMATION (10 Periods)

Spice Circuit Simulation, Discrete Transistor Modeling and Analysis, Gate Level Logic Simulation, Architecture Level Analysis, Data Correlation Analysis, Monte Carlo Simulation.

UNIT-III: LOW POWER CIRCUITS (11 Periods)

CIRCUIT ANALYSIS: Transistor and Gate Sizing, Equivalent Pin Ordering, Network Restructuring and Reorganization, Special latches and Flip flops.

LOGIC ANALYSIS: Gate Reorganization, Signal Gating, Logic Encoding, State Machine Encoding, Pre computation Logic.

UNIT-IV: SPECIAL TECHNIQUES (08 Periods)

Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing,Low Power Techniques for SRAM.

UNIT-V: ARCHITECTURE, SYSTEM & ADVANCED TECHNIQUES (9 Periods)

Power and Performance Management, Switching Activity Reduction, Adiabatic Computation, Pass Transistor Logic Synthesis, Asynchronous Circuit.

Total Periods: 45

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOK:

1. Gary Yeap, *Practical Low-Power Digital VLSI Design*, Springer Publication, 2012.

REFERENCE BOOKS:

1. A.P.Chandrakasan, R.W.Broadersen, *Low Power Digital CMOS Design*, Kluwer, Springer US, 2012.
2. Kaushik Roy, Sharat Prasad, *Low-Power CMOS VLSI Circuit Design*, Wiley Student Edition, 2009.

ADDITIONAL LEARNING RESOURCES:

https://nptel.ac.in/courses/106/105/106105034/
https://nptel.ac.in/courses/117/101/117101004/

CO-PO-PSO Mapping Table

Course Outcome	Program Outcomes												Program specific outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	2	2	-	-	-	3	-	-	-	-	3	-	-
CO2	3	3	2	2	-	-	-	3	-	-	-	-	3	-	-
CO3	3	2	3	2	1	-	1	3	-	-	-	-	3	-	-
CO4	3	2	2	2	3	-	1	3	-	-	-	-	3	-	-
Average	3	2.2	2.2	2	2	-	1	3	-	-	-	-	3	-	-
Course Correlation Level	**3**	**2**	**2**	**2**	**2**	**-**	**1**	**3**	**-**	**-**	**-**	**-**	**3**	**-**	**-**

Correlation Level: 3-High ; 2-Medium ; 1-Low

III B. Tech. - II semester

(19BM60404) MICROPROCESSORS AND MICROCONTROLLERS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: A Course on Switching Theory and Logic Design/Digital Logic Design.

COURSE DESCRIPTION: Architecture, Instruction set and programming of 8086; Programmable interfacing devices - architecture and programming; Interfacing Memory and I/O devices with 8086; 8051 Microcontroller - Architecture, programming, interrupts and applications.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze Architectural features and Instruction Set of 8086 for computing applications.
CO2: Analyze Techniques for Interfacing various peripherals to realize Microcomputer based systems.
CO3: Analyze Architectural features and Instruction Set of 8051 for control applications.
CO4: Design various embedded applications programming 8051 on-chip Resources and by interfacing various peripherals.

DETAILED SYLLABUS:

UNIT-I: 8086 ARCHITECTURE AND PROGRAMMING (10 Periods)

Microprocessor Evolution, Review of Intel 8085, 8086 internal Architecture - register organization, memory segmentation, memory organization; Introduction to programming the 8086 - Assembler directives, addressing modes, instruction set, simple programs, procedures and macros;

UNIT-II: 8086 INTERFACING AND INTERRUPTS (08 Periods)

Pin description, minimum & maximum mode operation of 8086, timing diagram. Interfacing memory (RAM and EPROM) to 8086. 8086 Interrupts - types and interrupt responses, Interrupt vector table, priority of interrupts; 8259 priority interrupt controller - architecture, system connections and cascading, initialization of 8529;

UNIT-III: PROGRAMMABLE DATA COMMUNICATION DEVICES (11 Periods)

Introduction to serial and parallel communication, methods of parallel data transfer. 8255 PPI - Internal architecture and system connections, operational modes and initialization, interfacing stepper motor, ADC, DAC, Optical Shaft Encoder; Methods of serial data transfer, 8251 USART - architecture and its initialization, sending and receiving characters; Serial communication standard - RS232C, USB; Architecture and operation of 8257 DMA controller.

UNIT-IV: MICROCONTROLLERS AND PROGRAMMING (08 Periods)

Microcontroller Vs. General purpose microprocessor, 8051/8052 Microcontroller – architecture, features, register organization, pin diagram, internal and external memories & their interfacing, instruction set, addressing modes, simple programs;

UNIT-V: 8051 INTERFACING **(08 Periods)**

Timer/Counters – Registers, modes and programming; Serial communication – registers, programming 8051 for serial communication; Interrupts – registers, programming; 8051 applications – Interfacing key board, LEDs and LCD;

Total Periods: 45

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOKS:

1. Douglas V. Hall, *Microprocessors and Interfacing: Programming and Hardware,* Tata McGraw-Hill, revised 2nd Edition, 2006.
2. Muhammad Ali Mazidi and Janice Gillispie Mazidi, *The 8051 Microcontroller and Embedded Systems,* Prentice Hall of India, 2000.

REFERENCE BOOKS:

1. A.K. Ray and K.M. Bhurchandi, *Advanced Microprocessors and Peripherals-Architecture, Programming and Interfacing,* Tata McGraw Hill, 2002 reprint.
2. Kenneth J. Ayala, *The 8051 microcontroller, Thomson Delmar learning,* 3rd Edition, 2004.

CO-PO-PSO Mapping Table

Course outcome	Program outcomes														
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO2	3	3	-	-	2	-	-	-	-	-	-	-	3	1	2
CO3	3	3	-	-	-	-	-	-	-	-	-	-	3	-	-
CO4	3	2	3	1	-	1	-	1	-	-	-	-	3	1	2
Average	3	2.5	3	1	2	1	-	1	-	-	-	-	3	1	2
Course Correlation Level	3	3	3	1	2	1		1	-	-	-	-	3	1	2

Correlation Level: 3-High ; 2-Medium ; 1-Low

III B. Tech. – II Semester

(19BM60431) **VLSI LAB**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	-	-	2	1

PRE-REQUISITES: A course on Switching Theory and Logic Design/ Digital Logic Design.

COURSE DESCRIPTION: Design and verification of various combinational & sequential digital circuits through source code.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze simplification methods in logic circuits and perform desired logical operations optimally using logic gates.

CO2: Design combinational circuits to perform arithmetic operations, data encoding and decoding, Multiplexing and Demultiplexing for engineering applications.

CO3: Design sequential circuits for realizing counters and registers using flip-flops.

CO4: Develop source code for Advanced Digital Design and perform functional verification.

CO5: Work independently or in teams to solve problems with effective Communication.

LIST OF EXERCISES/LIST OF EXPERIMENTS:

Part-A: Basic Digital Design

*(Minimum **SEVEN** experiments are to be conducted)*

Develop the source code for the following circuits and their test bench for verification. Also perform simulation, synthesis for given specifications

1. Buffer and basic gates.
2. Flip flops - RS, D, JK, T.
3. Adders and Subtractors.
4. 8-3 Encoder.
5. 3-8 Decoders.
6. 8x1 Multiplexer and 2x4 Demultiplexer.
7. Arithmetic and Logic Unit.
8. Synchronous &Asynchronous counter.
9. 4 Bit Comparator

Part-B: Advanced Digital Design (FPGA Implementation)

*(Minimum **THREE** Experiments are to be conducted)*

1. Write Verilog code for the design of 8-bit
   i. Carry Ripple Adder
   ii. Carry Look Ahead adder
   iii. Carry Save Adder

2. Write Verilog Code for the design of 8-bit
   i. Array Multiplier (Signed and Unsigned)
   ii. Booth Multiplier (Radix-4)
3. Write Verilog code for the design of 4/8-bit
   i. Universal Shift Register
   ii. Parity Generator
4. Write Verilog code for the design of 4/8-bit
   i. Pseudo Random Pattern Generator
   ii. LFSR

5. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence.
   Eg. 11101 (with and without overlap) any sequence can be specified

Note: (For the experiments listed above, students can make the following flow of study
-RTL synthesis
-creation of power Analysis
-use of I/O constrains)

REFERENCE BOOKS/LABORATORY MANUALS:

1. M. Morris Mano, *Digital Design*, Pearson Education, 5th edition, 2013.
2. Charles H. Roth, *Fundamentals of Logic Design*, Thomson Publications, 5th edition, 2004.
3. John F. Wakerly, *Digital Design Principles & Practices*, Pearson Education Asia, 4th Edition, 2008.
4. Stephen Brown and ZvonkoVramesic, *Fundamentals of Digital Logic with VHDL Design,* McGraw Hill, 2nd Edition, 2005.

SOFTWARE/Tools used:

CADENCE/SYNOPSYS/MENTOR GRAPHICS/TANNER or any other equivalent Tool
FPGA/CPLD Boards with Xilinx or any other equivalent

ADDITIONAL LEARNING RESOURCES:

1. http://www.vlab.co.in
2. https://swayam.gov.in

CO-PO-PSO Mapping Table

Course outcome	Program Outcomes												Program specific outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	-	2	3	1	-	-	-	-	-	-	3	-	-
CO2	3	1	3	2	3	1	-	-	-	-	-	-	3	-	-
CO3	3	2	3	2	3	1	-	-	-	-	-	-	3	-	-
CO4	3	2	3	2	3	1	-	-	-	-	-	-	3	-	-
CO5	-	-	-	-	-	-	-	-	3	3	-	-	-	-	-
Average	3	2	2.5	2	3	1	-	-	3	3	-	-	3	-	-
Course Correlation Level	**3**	**2**	**3**	**2**	**3**	**1**	**-**	**-**	**3**	**3**	**-**	**-**	**3**	**-**	**-**

Correlation Level: 3-High ; 2-Medium ; 1-Low

IV B. Tech. – I Semester
(19BM70401) **EMBEDDED SYSTEMS**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: A Course on Microcontrollers/Microprocessors and Microcontrollers.

COURSE DESCRIPTION: MSP430 Architecture; Instruction Set; Programming; On-Chip Resources; Communication with peripherals; Embedded system design approaches.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze MSP430 Architecture, Instruction Set, Addressing modes to develop programs for various control applications using Assembly and Embedded C.

CO2: Solve Problems by analyzing MSP430 On Chip Resources such as Timer, Clock System, Low Power Modes/techniques and Interrupt Structure.

CO3: Realize Mixed Signal Processing and Networking Applications, by analyzing on-Chip Resources such as Comparator, ADC, Temperature Sensor, PWM and Communication Peripherals.

CO4: Analyze Language, IDE Support, Processor IC & Design Technologies, and System Modeling Techniques to capture behavior of Embedded Prototype using suitable model.

DETAILED SYLLABUS:

UNIT-I: ARCHITECTURE OF MSP430 (09 Periods)

Embedded Systems – Introduction, MSP430 - Anatomy of microcontroller, Memory, Software, Pin out (MSP430G2553), Functional Block diagram, Memory, CPU, and Memory mapped input and output, Clock generator; Exceptions- Interrupts and Resets.

UNIT-II: PROGRAMMING MSP430 (09 Periods)

Development Environment, Aspects of C for Embedded Systems, Assembly Language, Register Organization, Addressing Modes, Constant Generator and Emulated Instructions, Instruction Set, Example programs- Light LEDs, Read input from a switch; Automatic Control-Flashing light by delay, use of subroutines and Functions; Basic Clock System, Interrupts and Low Power Modes.

UNIT-III: TIMERS AND MIXED SIGNAL SYSTEMS (09 Periods)

Timers - Watchdog Timer, RTC, Timer A, Measurement in capture mode, PWM generation; Mixed Signal Systems- Comparator A, ADC10 SAADC –Architecture, operation- Single Conversion, Temperature Sensor on ADC10, DTC in ADC10; ADC12 – Comparison with ADC10.

UNIT-IV: COMMUNICATION PERIPHERALS & PROTOCOLS (09 Periods)

MSP430 Communication Interfaces- USART,USCI, USI;
Communication Protocols- SPI, Inter-integrated Circuit Bus, USB, CAN

UNIT -V: EMBEDDED SYSTEM DESIGN **(09 Periods)**

Processor Technology, IC Technology, Design Technology, Tradeoffs.

Model VS.Language, System Modelling – Data Flow Model, FSM, FSMD, HCFSM, PSM, Concurrent Process Model & implementation.

Total Periods: *45*

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOKS:

1. John H. Davies, *MSP430 Microcontroller Basics*, Newnes Publications, 1st Edition, 2008.
2. Santanu Chattopadyay, Embedded System Design, PHI, 2010.
3. Frank Vahid, Tony D. Givargis, *Embedded System Design – A Unified Hardware/Software Introduction,* John Wiley, January 2006

REFERENCE BOOKS:

1. Chris Nagy, *Embedded Systems Design using the TI MSP30 Series*, Newnes Publications, October 2003.
2. JorgeonStaunstrup, Wayne Wolf, *Hardware/Software Co-design Principles and Practice*, Springer 2009.
3. Patrick R Schamont, *A Practical Introduction to Hardware/Software Co-design, Springer publications*, January 2010

CO-PO-PSO Mapping Table

Course outcome	Program outcomes												Program specific outcomes		
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**	**PSO3**
CO1	3	3	-	1	-	-	-	-	-	-	-	-	2	1	-
CO2	3	3	2	3	2	2	-	-	-	-	-	-	2	2	-
CO3	3	3	3	2	2	2	-	2	-	-	-	-	1	2	2
CO4	3	3	2	2	2	2	-	2	-	-	-	-	1	1	1
Average	3	3	2.3	2	2	2	-	2	-	-	-	-	1.5	1.5	1.5
Course Correlation Level	**3**	**3**	**3**	**2**	**2**	**2**	**-**	**2**	**-**	**-**	**-**	**-**	**2**	**2**	**2**

Correlation Level: 3-High ; 2-Medium ; 1-Low

IV B. Tech. – I Semester

(19BM70402) **REAL TIME SYSTEMS**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: Courses on Microcontrollers/ Microprocessors and Microcontrollers & Embedded Systems.

COURSE DESCRIPTION: Real Time Systems Modeling; Scheduling Approaches ;Multiprocessor and Distributed Scheduling Algorithms; Fault Tolerant Systems; Real Time Operating Systems.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze Real Time System Characterization, Workload and Resource management algorithms and apply suitable techniques to model hard and soft real time systems.
CO2: Solve scheduling problems and apply suitable techniques in constrained RT systems by Surveying various Real Time scheduling approaches for uniprocessor, Multiprocessor and distributed environments.
CO3: Evaluate appropriate Fault tolerant techniques and apply them to design fail safe RT systems.
CO4: Implement Efficient Real Time Systems porting suitable operating system on to hardware by Investigating POSSIX standard Kernel structure, services and Kernel objects.

DETAILED SYLLABUS:

UNIT-I: MODELING OF REAL TIME SYSTEMS (09 Periods)

Hard Vs Soft Real Time Systems, A Reference Model of Real Time Systems- Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency. Functional Parameters, Resource Parameters of Jobs and Parameters of Resources, Scheduling hierarchy.

UNIT-II: APPROACHES TO REAL TIME SCHEDULING (09 Periods)

Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs Static Systems, Effective Release Times and Dead Lines, Optimality and Non-optimality of EDF and LST algorithms, Challenges in Validating Timing Constraints in Priority Driven Systems, Offline Vs Online Scheduling.

UNIT-III: SCHEDULING REAL TIME TASKS IN MULTIPROCESSOR AND DISTRIBUTED SYSTEMS (09 Periods)

Multiprocessor task allocation, Dynamic allocation of tasks, Fault tolerant scheduling of tasks, Clocks in distributed Real Time Systems, Centralized clock distribution, Distributed clock synchronization.

UNIT-IV: FAULT TOLERANCE TECHNIQUES (09 Periods)

Introduction, Failures- Causes, Types, Detection. Fault and Error Containment, Redundancy- Hardware, Software, Time, Integrated Failure Handling.

UNIT-V: OPERATING SYSTEMS **(09 Periods)**

Overview- Threads and Tasks, the Kernel. Time Services and Scheduling Mechanisms, Basic Operating System Functions- Communication and Synchronization, Event Notification and Software Interrupt Memory Management, I/O and Networking. Processor Reserves and Resource Kernel, Capabilities of Commercial Real Time Operating Systems.

Total Periods: 45

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOKS:

1. Jane W.S. Liu, "*Real Time Systems*", Pearson Education, 1st Edition, 2006.
2. Rajib Mall, "*Real Time Systems-Theory and Practice*", Pearson Education India,1st Edition, Nov.2012.
3. C. M. Krishna, Kang G Shin, "*Real Time Systems*", MCgraw-Hill Series, Dec. 1996.

REFERENCE BOOKS:

1. Phillip A. Laplante and Seppo J. Ovaska, "*Real-Time Systems Design and Analysis: Tools for the Practitioner"*, Wiley-IEEE Press, 4th edition, Nov. 2011.
2. Hermann Kopetz, "*Real-Time Systems: Design Principles for Distributed Embedded Applications* ", Springer; 2nd Edition, 2011.

CO-PO-PSO Mapping Table

Course Outcome	Program Outcomes												Program specific outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	2	2	-	-	-	3	-	-	-	-	3	-	-
CO2	3	3	2	2	-	-	-	3	-	-	-	-	3	-	-
CO3	3	2	3	2	1	-	1	3	-	-	-	-	3	-	-
CO4	3	2	3	2	3	-	1	3	-	-	-	-	3	-	-
Average	3	2.5	2.5	2	2	-	1	3	-	-	-	-	3	-	-
Course Correlation Level	**3**	**3**	**3**	**2**	**2**	**-**	**1**	**3**	**-**	**-**	**-**	**-**	**3**	**-**	**-**

Correlation Level: 3-High ; 2-Medium ; 1-Low

IV B. Tech. – I Semester

(19BM70403) SYSTEM-ON-CHIP DESIGN AND VERIFICATION

Int.	Ext.	Total	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: A Course on VLSI Design.

COURSE DESCRIPTION: System on Chip Design (SOC) Process; System level Design Issues; Test Strategies; Macro Design and Verification; Reusable Macros; System on Chip Verification; Communication Architectures for SoCs.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Demonstrate various SoC Design aspects and issues in low power and high speed Implementations.
CO2: Analyze the Macro Design Process to solve issues in usage of hard macros and Develop reusable macros for system integration.
CO3: Analyze verification methods at system level, block level and Hardware/Software Co-verification to reduce the test time.
CO4: Apply various communication architectures to design energy efficient systems.

DETAILED SYLLABUS:

UNIT-I: SYSTEM ON CHIP DESIGN PROCESS (08 Periods)

A canonical SoC Design, SoC Design flow- waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification, System Design process, System level design issues - Soft IP Vs Hard IP, Design for timing closure - Logic design issues, Verification strategy, Onchip buses and interfaces, Design for Low Power, Manufacturing test strategies.

UNIT-II: MACRO DESIGN PROCESS (07 Periods)

Overview of IP Design, planning and Specification, Macro Design and Verification, Soft Macro Productization, Developing hard macros - Design issues for hard macros, Model Development for Hard Macros. System Integration with reusable Macros.

UNIT-III: SoC VERIFICATION - I (12 Periods)

Technology Challenges, Verification technology options, Verification methodology, Testbench Creation, Testbench Migration, Verification languages, Verification IP Reuse, Verification approaches, Verification and Device Test, Verification plans, Bluetooth SoC. System level verification – System Design, System Verification.
Block level verification – IP Blocks, Block Details of Bluetooth SoC, Lint Checking, Formal Model Checking, Functional Verification/Simulation, Protocol Checking, Directed Random Testing, Code Coverage Analysis

UNIT-IV: SoC Verification - II (12 Periods)

Hardware/Software Co-verification- HW/SW Co-verification Environment, Emulation, soft or virtual Prototypes, Co-verification, UART Co-verification, Rapid Prototype Systems, Software Testing. Static netlist verification, Physical Verification and Design Signoff, Introduction to VMM (Verification Methodology Manual), OVM(Open Verification Methodology) and UVM (Universal Verification Methodology).

UNIT-V: DESIGN OF COMMUNICATION ARCHITECTURES FOR SoCs (06 Periods)
On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures-Communication architecture tuners. Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification**.**

Total Periods: *45*

Topics for Self-Study are provided in the Lesson Plan

TEXT BOOKS:

1. Michael Keating, Pierre Bricaud, "*Reuse Methodology manual for System On A Chip Designs*", Kluwer Academic Publishers, Springer US, 3rd Edition, 2007.
2. Prakash Rashinkar, Peter Paterson and Leena Singh, "*SoC Verification Methodology and Techniques"*, Kluwer Academic Publishers, Springer US, 2013.
3. A.A. Jerraya, W.Wolf, "*Multiprocessor Systems-on-chips*", M K Publishers, Elsevier Science, 2005.

REFERENCE BOOKS:

1. William K. Lam, "*Hardware Design Verification: Simulation and Formal Method based Approaches"*, Prentice Hall, 1st Edition, 2005.
2. Farzed Nekoogar, Faranak Nekoogar, "*From ASICs to SOCs: A Practical Approach*", China Machine Press, 2006.

CO-PO-PSO Mapping Table

Course outcome	Program Outcomes												Program specific outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	2	-	1	-	-	-	-	-	-	-	-	3	-	-
CO2	3	3	2	1	-	-	-	-	-	-	-	-	3	-	-
CO3	3	3	2	1	-	-	-	-	-	-	-	-	3	-	-
CO4	3	1	2	2	3	-	-	-	-	-	-	-	3	-	-
Average	3	2.2	2	1.2	3	-	-	-	-	-	-	-	3	-	-
Course Correlation Level	3	2	2	1	3	-	-	-	-	-	-	-	3	-	-

Correlation Level: 3-High ; 2-Medium ; 1-Low

IV B. Tech. – I Semester

(19BM70431)**EMBEDDED SYSTEMS LAB**

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	-	-	2	1

PRE-REQUISITES: A Course on Microcontrollers.

COURSE DESCRIPTION: Familiarization using IDE – CCS, Energia; Instruction Set usage; GPIO – programming; Watchdog timer; Timer, ADC, Comparator – Programming; Low Power Modes demonstration; PWM generation – Speed Control of DC Motor; Networking MSPs.

COURSE OUTCOMES: After successful completion of this course, the students will be able to:

CO1: Analyze MSP430 Architecture, Instruction Set and Demonstrate Competence in developing programs using Assembly and Embedded C.
CO2: Solve various Problems using CCS and Energia IDE effectively by evaluating various on-chip resources.
CO3: Develop programs to realize control applications such as Speed control of DC Motor, Reading Ambient Temperature by investigating various interfacing techniques.
CO4: Survey usage of MSP430 for Mixed Signal Processing and IOT Applications to establish communication deploying various protocols.
CO5: Work independently and in teams to solve problems with effective Communication.

LIST OF EXERCISES/LIST OF EXPERIMENTS:
(Minimum Ten Experiments to be done)

1. Introduction to MSP430 launch pad and Programming Environment.
2. Practice on usage of Instruction Set
3. Read input from switch and Automatic control/flash LED (software delay).
4. Interrupts programming example using GPIO.
5. Configure watchdog timer in watchdog & interval mode.
6. Configure timer block for signal generation (with given frequency).
7. Read Temperature of MSP430 with the help of ADC.
8. Test various Power Down modes in MSP430.
9. Generation of Pulse Width Modulation.
10. Use Comparator to compare the signal threshold level.
11. Speed Control of DC Motor
12. Master slave communication between MSPs using SPI.
13. Networking MSPs using Wi-Fi.

REFERENCE BOOKS/LABORATORY MANUALS:

1. John H Davies, *MSP430 Microcontrollers Basics*, Newnes Publishers, 1st Edition, 2008.
2. C P Ravikumar, *MSP430 Microcontrollers in Embedded System Projects*, Elite Publishing House , 1st Edition, 2012.

SOFTWARE/Tools used:

Code Composer Studio Version 6, Energia, MSP430 launch pads, Wi-Fi booster pack.

CO-PO-PSO Mapping Table

Course Outcome	Program Outcomes												Program specific outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO 1	PSO2	PSO 3
CO1	3	3	1	2	2	-	-	-	-	-	-	-	2	2	-
CO2	3	3	2	3	2	1	1	-	-	-	-	1	2	2	-
CO3	3	3	3	2	1	1	-	-	-	-	-	2	2	3	-
CO4	3	3	3	2	1	1	1	2	-	-	-	2	-	2	3
C05	-	-	-	-	-	-	-	-	3	3	-	-	-	-	-
Average	3	3	2.2	2.2	1.5	1	1	2	3	3	-	1.6	2	2.2	3
Course Correlation Level	**3**	**3**	**2**	**2**	**2**	**1**	**1**	**2**	**3**	**3**	**-**	**2**	**2**	**2**	**3**

Correlation Level: 3-High ; 2-Medium ; 1-Low