SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, Tirupati

Department of Electronics and Communication Engineering

Supporting Document for 1.1.3

Courses having focus on

Employability/ Entrepreneurship/ skill Development

Program: M.Tech.- VLSI

Regulations : SVEC-14

The Courses (with course outcomes) under SVEC-14 Regulations which focus on ***employability/ entrepreneurship/ skill development*** are highlighted with the following colours.

Skill

Employability

Entrepreneurship

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(Autonomous)

DEPARTMENT OF ECE

COURSE STRUCTURE for M.Tech. (VLSI)

I – SEMESTER

S. No.	Course Code	Course Title	Periods per week			C	Scheme of Examination Max. Marks		
			L	T	P		Int.	Ext.	Total
1.	14MT15701	Analog IC Design	4	-	-	4	40	60	100
2.	14MT15702	Computational Techniques in Microelectronics	4	-	-	4	40	60	100
3.	14MT15703	Device Modeling	4	-	-	4	40	60	100
4.	14MT15704	Digital IC Design	4	-	-	4	40	60	100
5.	14MT15705	IC Fabrication	4	-	-	4	40	60	100
6.		**Elective-I**							
	14MT15706	Advanced Digital Signal Processing	4	-	-	4	40	60	100
	14MT15707	FPGA Applications							
	14MT15708	Low Voltage Analog Circuit Design							
	14MT15709	ULSI Technology							
7.	14MT10310	Research Methodology	3	-	-	3	40	60	100
8.	14MT15721	Analog and Digital IC Design Lab.	-	-	4	2	25	50	75
		Total:	**27**	**-**	**4**	**29**	**305**	**470**	**775**

II-Semester

S. No.	Course Code	Course Title	Periods per week			C	Scheme of Examination Max. Marks		
			L	T	P		Int.	Ext.	Total
1.	14MT25701	Physical Design Automation	4	-	-	4	40	60	100
2.	14MT25702	Low Power VLSI Design	4	-	-	4	40	60	100
3.	14MT25703	Mixed Signal Design	4	-	-	4	40	60	100
4.	14MT25704	RF IC Design	4	-	-	4	40	60	100
5.	14MT25705	Testing and Testability	4	-	-	4	40	60	100
6.		**Elective-II**							
	14MT25706	ASIC Design	4	-	-	4	40	60	100
	14MT25707	Co-Design							
	14MT25708	DSP Processors							
	14MT25709	Wireless Sensor Networks							
7.	14MT25721	Mixed Signal Lab.	-	-	4	2	25	50	75
8.	14MT25722	Seminar	-	-	-	2	-	50	50
		Total:	**24**	**-**	**4**	**28**	**265**	**460**	**725**

III-Semester

S. No.	Course Code	Course Title	Periods per week			C	Scheme of Examination Max. Marks		
			L	T	P*		Int.	Ext.	Total
1	14MT35721	Project Work – Phase I	-	-	-	4	40	-	40
		Total:	**-**	**-**	**-**	**4**	**40**	**-**	**40**

*Fulltime Project Work

IV-Semester

S. No.	Course Code	Course Title	Periods per week			C	Scheme of Examination Max. Marks		
			L	T	P*		Int.	Ext.	Total
1	14MT45721	Project Work – Phase II	-	-	-	12	40	120	120
		Total:	**-**	**-**	**-**	12	**40**	**120**	**160**

*Fulltime Project Work

Total Credits: 73 **Total Marks: 1700**

SREE VIDYANIKETHAN ENGINEERING COLLEGE (Autonomous)

M. Tech. (VLSI)-I Semester
(14MT15701) ANALOG IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
Courses on Semiconductor Devices and Circuits and Linear IC Applications at UG Level

COURSE DESCRIPTION:
Device physics; Characteristics of amplifiers; Feedback circuits and operational amplifiers; Stability and frequency compensation of operational amplifiers; Switched capacitor circuits.

COURSE OUTCOMES: On completion of course, the student will be able to

- CO1. Demonstrate advanced knowledge in
  - Current Mirrors
  - Effect of Loading in Feedback Circuits
  - One stage operational Amplifiers
  - Switched-Capacitor Circuits
- CO2. Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
- CO3. Solve engineering problems for feasible and optimal solutions in the core area of analog ICs.
- CO4. Apply appropriate techniques to engineering problems in the filed of analog IC design.

DETAILED SYLLABUS

UNIT- I:

Basic MOS Device Physics: (Periods:14)
General Considerations, MOS I/V Characteristics, Second-Order Effects, MOS Device Models.

Single Stage Amplifiers:
Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential Amplifiers and Current Mirrors.

UNIT- II: FREQUENCY RESPONSE AND NOISE CHARACTERISTICS OF AMPLIFIERS (Periods:07)
Frequency Response-General Considerations, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential pair. Noise-Statistical Characteristics of Noise, Noise in Single Stage Amplifiers, Noise in Differential Pairs.

UNIT- III: FEEDBACK CIRCUITS AND OPERATIONAL AMPLIFIERS (Periods:12)
Feedback Circuits - General considerations, Feedback Topologies, effect of loading, Effect of Feedback on Noise.

Operational Amplifiers - General considerations, One-stage Op Amps, Two - stage Op Amps, Gain boosting, Input range limitations, slew rate, power supply rejection, Noise in Op Amps.

UNIT- IV:

Stability and Frequency Compensation: (Periods:08)

General considerations, Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps, Other Compensation Techniques.

Bandgap References:

Supply-Independent Biasing, Temperature-independent References, PTAT Current Generation, Constant - Gm Biasing, Speed and Noise Issues.

UNIT-V: INTRODUCTION TO SWITCHED–CAPACITOR CIRCUITS

(Periods:09)

General Considerations, Sampling Switches, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitors Common-Mode Feedback.

Total Periods: 51

TEXT BOOKS:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata-McGraw-Hill, 2002.

REFERENCE BOOKS:

1. D.A. John & Ken Martin, "Analog Integrated Circuit Design", John Wiley, 1997.
2. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.

M. Tech. (VLSI)-I Semester
(14MT15702) COMPUTATIONAL TECHNIQUES FOR MICROELECTRONICS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Mathematics at UG Level.

COURSE DESCRIPTION:
Computational techniques for linear and non-linear systems; Initial and final value problems; Finite volume method based on differential equations; Error estimation and refinement algorithms; Performance and yield estimation algorithms.

COURSE OUTCOMES: On successful completion of this course the students will be able to

CO1: Demonstrate in-depth knowledge in
- Computation Tools.
- FDM, FEM, FVM.
- Grid Generation.
- Refinement Algorithms.
- Errors in Meshing.
- Application to device and process simulation.

CO2: Analyze the errors of Computational tools and judge independently the best suited Tool for fast Computation of simulation for conducting research in CAD Tools design.

CO3: Solve problems of Meshing, Grid Generation to improve speed and accuracy of CAD Tools.

CO4: Apply appropriate techniques, resources and tools to engineering activities to obtain fast and accurate designs.

CO5: Contribute positively to multidisciplinary scientific research in design and development of CAD Tools suited for wide range of applications.

DETAILED SYLLABUS:

UNIT I: BASIC COMPUTATION TOOLS (Periods:14)
Linear systems and matrices – matrix formalities, condition of matrix systems, techniques for matrix solution, mixed boundary condition. Nonlinear Systems – scalar equations, matrix equations. Approximation, interpolation, curve fitting, Numerical Integration.

UNIT II: COMPUTATIONAL TOOLS FOR APPLICATIONS (Periods:09)
Finite difference techniques, Initial Value problems, Energy Methods and Minimization, finite Element methods, dynamic methods in applied mechanics.

UNIT III: ADVANCED COMPUTATIONAL TOOLS (Periods:08)
Method of characteristics – classification of partial Differential equations, Investigations in Engineering, Finite volume methods – Direct Analysis.

UNIT IV: GRID GENERATION AND ERROR ESTIMATES (Periods:10)
Grid generation, Triangulation, errors and mesh Selection, Refinement Algorithms, Mesh Redistribution, Moving Grids.

UNIT V: APPLICATIONS TO DEVICE AND PROCESS SIMULATION (Periods:11)
Applications to device and process simulation, Layout algorithms, Yield estimation algorithms, Symbolic analysis and Synthesis of Analog ICs.

Total periods: 52

TEXT BOOKS:

1. Herbert Koenig,"Modern Computational methods", CRC Press, 1988.
2. Graham F.carey, " Computational Grids: generations, adaptation & Solution Strategies", CRC Press, 1997.
3. Naveed A. Sherwani,"Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 1993.algorithms

REFERENCE BOOKS:

1. L.Pallage, R.Rohrer And C.Visweswaraiah, "Electronic Circuit and System Simulation Methods", McGraw Hill, 1995.

M. Tech. (VLSI)-I Semester
(14MT15703) DEVICE MODELING

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Semiconductor Devices and Circuits at UG Level

COURSE DESCRIPTION:
Device physics; Short channel effects; Static and dynamic behavior of MOS transistor; Small and large signal modeling of MOS transistor at various frequencies.

COURSE OUTCOMES:
On successful completion of this course the students will be able to

CO1: Demonstrate in-depth knowledge in
- Static and Dynamic Characteristics
- Threshold Variations
- Effects of MOS Layers
- Modeling at low and High Frequencies.

CO2: Analyze complex engineering problems critically for conducting research in MOS device structures.

CO3: Solve engineering problems with wide range of solutions in different MOSFET technologies.

CO4: Apply appropriate techniques, resources and tools to engineering activities in modeling MOS structures.

DETAILED SYLLABUS:

UNIT-I: BASIC DEVICE PHYSICS-I (Periods:12)

Two Terminal MOS Structure: Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance; C-V Characteristics.

Three Terminal MOS Structure: Contacting the inversion layer, Body effect, Regions of inversion, Pinch-off voltage.

UNIT-II: BASIC DEVICE PHYSICS-II (Periods:14)

Four Terminal MOS Transistor: Transistor regions of operation, general charge sheet models, regions of inversion in terms of terminal voltage, strong inversion, weak inversion, moderate inversion, interpolation models, effective mobility, temperature effects, breakdown p-channel MOS FET, enhancement and depletion type, model parameter values, model accuracy .

UNIT-III: (Periods:14)

MOS Transistor with Ion-Implanted Channels: Enhancement of nMOS, Depletion nMOS, Enhancement pMOS.

Small dimension effects: Channel length modulation, barrier lowering, two dimensional charge sharing and threshold voltage, punch-through, carrier velocity saturation, hot carrier effects, scaling, effects of surface and drain series resistance, effects due to thin oxides and high doping. Sub threshold regions, Short channel effects.

UNIT-IV: MOS TRANSISTOR IN DYNAMIC OPERATION (Periods:06)

Large Signal modeling: Quasi static operation, Terminal currents in Quasi static operation, Evaluation of Charges in Quasi static operation, Transit time under DC conditions, Limitations of Quasi static Model, Non Quasi static Analysis.

UNIT-V: SMALL SIGNAL MODELING FOR LOW, MEDIUM AND HIGH FREQUENCIES (Periods:08)

low, Medium frequency small signal model for the intrinsic part, Small signal model for Extrinsic Part, A complete Quasi static Model, Y-Parameter models, Non Quasi static Models.

Total Periods: 54

TEXT BOOK:

1. Y. Tsividis, "Operations and Modeling of the MOS Transistor", 2nd edition, Oxford university Press.

REFERENCE BOOKS:

1. Trond Ytterdal, Yuhua Cheng &Tor A. Fjeldly "Device Modeling for Analog and RF CMOS Circuit Design" Wiley Publication, 2003.
2. Donald A Neamen & Dhrubes Biswas "Semiconductor Physics and Devices" Special Indian Edition, 2012.

M. Tech. (VLSI)-I Semester
(14MT15704) DIGITAL IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Digital IC Applications and VLSI Design at UG Level.

COURSE DESCRIPTION:
Design styles and characteristics of CMOS digital circuits; Transistor sizing and memory design; Design strategies; Layout design rules; Design of sub-systems.

COURSE OUTCOMES:
On successful completion of this course the students will be able to

CO1: Demonstrate advanced knowledge in
- Static and dynamic characteristics of CMOS.
- Alternative CMOS Logics
- Transistor sizing
- Adders Design
- Design rules to develop layouts
- Estimation of Delay and Power

CO2: Analyze complex engineering problems critically in the domain of CMOS Digital Integrated Circuits for conducting research.

CO3: Solve engineering problems for feasible and optimal solutions in the core area of CMOS Digital ICs.

CO4: Apply the CMOS Digital IC concepts for usage of modern CAD tools and their Limitations.

DETAILED SYLLABUS:

UNIT I: CMOS INVERTERS CHARACTERSTICS AND DESIGN STYLES (Periods:09)
Static and Dynamic characteristics, Static and Dynamic CMOS design- Domino and NORA logic - Combinational and Sequential circuits.

UNIT II: **HIGH SPEED NETWORK AND MEMORY DESIGN (Periods:09)**
Methods of Logical Effort for transistor sizing -Power consumption in CMOS Gates, Low power CMOS design. CMOS Memory design – SRAM, DRAM.

UNIT III: **DESIGN METHODOLOGY AND TOOLS (Periods:10)**
Introduction, Structured Design Strategies, Design Methods, Design Flows, Design Economics, Data Sheets and Documentation.

UNIT IV: **LAYOUT DESIGN RULES (Periods:11)**
Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load.

UNIT V: **SUBSYSTEM DESIGN PROCESS** **(Periods:11)**

General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Multipliers, modified Booth's algorithm.

TEXT BOOKS:

1. Eugene D Fabricus, "Introduction to VLSI Design, "McGraw Hill International Edition, 1990.
2. Kamran Eshranghian, Douglas A.Puknell and Sholh Eshranghian"Essential of VLSI Circuits and Systems", PHI , 1st edition, 2005.
3. Neil H. E. Weste, David Money Harris,"CMOS VLSI Design-A Circuit and Systems Perspective", Pearson 4th Edition,2011.

REFERENCE BOOKS:

1. John P.Uyemura, "Introduction to VLSI Circuits and Systems", Wiley Edition, 2002.
2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", McGraw Hill, 2nd edition, 1999.
3. Jan M Rabaey, "Digital Integrated Circuits-A Design Perspective", Prentice Hall, 1st edition, 1997.

M.Tech. (VLSI) - I Semester
(14MT15705) IC FABRICATION

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Engineering Physics, VLSI Design at UG Level

COURSE DESCRIPTION:
Fabrication process – Crystal growth, Wafer preparation, Epitaxial growth, Oxidation, Lithography, Etching, Deposition, Diffusion, Ion Implantation, Metallization and Packaging of VLSI Devices.

COURSE OUTCOMES
On completion of the course, the students will be able to

CO1. Demonstrate in-depth knowledge in
- Wafer preparation.
- Lithography and Etching.
- Diffusion process.
- Assembly Techniques and Packaging.

CO2. Analyze IC fabrication methodologies and evaluate component effects on IC design for VLSI and ULSI domain.

CO3. Solve engineering problems by proposing potential solutions leading to better IC chip designs.

DETAILED SYLLABUS

UNIT-I: CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION. (Periods:12)

Clean room and safety requirements, Electronic grade silicon – Basic steps in IC fabrication-crystal plane and orientation – Defects in the lattice –Czochralski crystal growing – silicon shaping – Processing consideration – Vapour phase epitaxy –Liquid phase epitaxy-selective epitaxy- Molecular beam epitaxy - Epitaxial Evaluation – Growth mechanism and kinetics – Thin oxides – Oxidation Techniques and systems – Oxide properties – Redistribution of dopants at interface – Oxidation of polysilicon – Oxidation induced effects.

UNIT-II: LITHOGRAPHY AND RELATIVE PLASMA ETCHING (Periods:10)

Mask Making – Optical lithography – Electron lithography – X-ray lithography – Ion lithography – Plasma properties– Feature size control and Anisotropie Etch mechanism – Lift off Techniques – Plasma reactor – Fl2 &Cl2 based etching – Relative plasma etching Techniques and Equipments.

UNIT-III: DEPOSITION, DIFFUSION, ION IMPLANTATION (Periods:10)

Deposition process – polisilicon - plasma assisted deposition – models of diffusion in solids – Fick's one dimensional diffusion equation – Atomic diffusion mechanism – measurement techniques – Range theory – Carrier recovery due

to annealing - Implantation equipment – Annealing Shalloe junction – high energy implantation – Physical vapour deposition – patterning.

UNIT- IV: METALLIZATION (Periods:10)

Metallization applications – metallization choices – Patterning – Metallization problems – New role of metallization-metallization systems – sputtering – problems associated with Al – Cu interconnect – Comparison of RC delay of Polysilicon, Al.

UNIT-V: ANALYTICAL, ASSEMBLY TECHNIQUES & PACKAGING OF VLSI DEVICES (Periods:10)

Analytical beams – Beams specimen interaction – Chemical methods – package types – baking design considerations – VLSI assembly technology – Package Fabrication Technology.

Total periods: 52

TEXT BOOKS

1. S.M.Sze "VLSI Technology", Tata Mcgraw Hill, 2nd edition, 1988.

REFERENCES BOOKS

1. Sorab. K. Gandhi "VLSI Fabrication and Principles", John wiley and sons, 1983.
2. Amar Mukherjee "Introduction to NMOS & CMOS VLSI system Design", Prentice Hall, 1986.
3. Mccanny and J.C.White "VLSI Technology and design", Academic Press, 1987.
4. Dasgupta "VLSI Technology", Pearson Education Pvt Ltd 2001.

M. Tech. (VLSI) - I Semester (Elective-I)
M. Tech. (CMS) - I Semester
(14MT15706) ADVANCED DIGITAL SIGNAL PROCESSING

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES: Courses on Digital Signal Processing at UG level.

COURSE DESCRIPTION:
Design of digital filter banks; Power spectral estimation; Digital signal processing algorithms; DSP applications.

COURSE OUTCOMES:
On successful completion of this course the students will be able to

CO1. Demonstrate advanced knowledge in
- Filter banks and Wavelets
- Efficient power Spectral Estimation Techniques.
- Adaptive filters.
- Applications of Multirate signal processing

CO2. Analyze complex engineering problems critically for conducting research in Adaptive filter design.

CO3. Solve engineering problems by designing computationally efficient DSP algorithms for feasible and optimal solutions in digital signal processing field.

CO4. Contribute to scientific research in signal processing and inter disciplinary areas like cellular mobile communications, multirate signal processing and spectral analysis.

DETAILED SYLLABUS:

UNIT I: MULTIRATE FILTER BANKS (Periods:12)
Decimation, Interpolation, Sampling rate conversion by a rational factor I/D, Multistage Implementation of sampling rate conversion. **Digital Filter Banks**: Two-Channel Quadrature-Mirror Filter Bank, Elimination of aliasing, condition for Perfect Reconstruction, Polyphase form of QMF bank, Linear phase FIR QMF bank, IIR QMF bank , Perfect Reconstruction Two-Channel FIR QMF Bank .

UNIT II: POWER SPECTRAL ESTIMATIONS (Periods:11)
Estimation of spectra from finite duration observation of signals, **Non-Parametric Methods**: Bartlett, Welch, Blackmann & Tukey methods. Performance Characteristics of Nonparametric Power Spectrum Estimators, Computational Requirements of Nonparametric Power Spectrum Estimates.

UNIT III: PARAMETRIC METHODS OF POWER SPECTRAL ESTIMATION (Periods:11)
Autocorrelation & Its Properties, Relation between auto correlation & model parameters, Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT IV: DSP ALGORITHMS (Periods:10)

Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNITV: APPLICATIONS OF DIGITAL SIGNAL PROCESSING (Periods:11)

Digital cellular mobile telephony, Adaptive telephone echo cancellation, High quality A/D conversion for digital Audio, Efficient D/A conversion in compact hi-fi systems, Acquisition of high quality data, Multirate narrow band digital filtering, High resolution narrowband spectral analysis.

Total periods: 55

TEXT BOOKS:

1. John G. Proakis, Dimitris G. Manolakis, *Digital signal processing, principles, Algorithms and applications,* Prentice Hall, 4th Edition, 2007.
2. Sanjit K Mitra, "*Digital signal processing, A computer base approach",* McGraw-Hill Higher Education, 4th Edition, 2011.

REFERENCE BOOKS:

1. Emmanuel C Ifeacher Barrie. W. Jervis, "*DSP-A Practical Approach*", Pearson Education, 2nd Edition, 2002.
2. A.V. Oppenheim and R.W. Schaffer, "*Discrete Time Signal Processing",* PHI, 2nd Edition, 2006.

M. Tech. (VLSI)-I Semester (Elective-I)
(14MT15707) FPGA APPLICATIONS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
Course on VLSI Design at UG Level

COURSE DESCRIPTION:
Families of Field Programmable Gate Arrays; Embedded processors using FPGA; Applications of FPGAs - Motor control, FIR and IIR filters.

COURSE OUTCOMES: On completion of the course, student will be able to
CO1. Demonstrate in-depth knowledge in
- FPGAs Design & Architecture.
- Motor Control with FPGAs.
- FIR and IIR Digital Filter implementation with FPGAs.
- FPGA Fabric Immersed Processors.

CO2. Analyze complex engineering problems critically in Programmable digital systems.
CO3. Develop skills to solve the problems in placement and routing of FPGAs.
CO4. Apply appropriate techniques to engineering problems in the design of FPGAs.

DETAILED SYLLABUS

UNIT- I:
Introduction to Field Programmable Gate Arrays (FPGA): (Periods:10)
Evolution of Programmable Devices, About FPGAs, Applications of FPGAs. Programming Technologies in FPGAs.
Xillinx and Actel FPGAs:
Xilinx FPGAs –XC2000, XC3000 and XC4000.Actel FPGAs – Actel ACT-1 and Actel ACT-2. Altera FPGAs, Plessey FPGA, Advanced Micro Devices (AMD) FPGA. FPGA Design Flow. Technology Mapping for FPGAs-Logic Synthesis and Lookup Table Technology Mapping.

UNIT- II: FPGA-BASED EMBEDDED PROCESSOR (Periods:07)
Hardware–Software Task Partitioning, FPGA Fabric Immersed Processors, Interfacing Memory to the Processor, Interfacing Processor with Peripherals, Design Re-use Using On-chip Bus Interface, Creating a Customized Microcontroller.

UNIT- III: MOTOR CONTROL USING FPGA (Periods:09)
Introduction to Motor Drives, Digital Block Diagram for Robot Axis Control-Position Loop, Speed Loop and Power Module. Case Studies for Motor Control-Stepper Motor Controller, Permanent Magnet DC Motor, Brushless DC Motor and Permanent Magnet Rotor (PMR). Prototyping Using FPGAs.

UNIT- IV: FIR DIGITAL FILTERS USING FPGA (Periods:14)

Digital Filters, FIR Filter-FIR Filter with Transposed Structure, Symmetry in FIR Filters and Linear-phase FIR Filters. Designing FIR Filters-Direct Window Design Method and Equiripple Design Method. Constant Coefficient FIR Design-Direct FIR Design, FIR Filter with Transposed Structure and FIR Filters Using Distributed Arithmetic.

UNIT- V: IIR DIGITAL FILTERS USING FPGA (Periods:10)

Introduction to IIR, IIR Digital Filter, IIR Coefficient Computation, IIR Filter Implementation-

Finite wordlength effects and Optimization of the Filter Gain Factor. Fast IIR Filter-Time domain Interleaving and Clustered and Scattered Look-Ahead Pipelining.IIR Decimator Design and Parallel Processing.

Total periods:50

TEXT BOOKS:

1. S.Brown, R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array", Kluwer Publication, 1992.
2. Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable Gate Arrays", Springer, 2009.
3. Uwe Meyer-Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer Series, 3rd Edition, 2007.

REFERENCE BOOKS:

1. S.Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.

M. Tech. (VLSI)-I Semester (Elective-I)
(14MT15708) LOW VOLTAGE ANALOG CIRCUIT DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
Basic methods for low voltage design; FGMOS devices and their applications; Low power SOC design; RF CMOS circuits – Considerations and design of receiver components.

COURSE OUTCOMES:
On successful completion of this course the students will be able to

CO1: Demonstrate in-depth knowledge in
- Low Voltage Techniques.
- FGMOS Device and Design Techniques.
- Light Weight Embedded Systems.
- Low Power SOC Design.
- Analog RF CMOS Circuits
- Low power architecture & Systems.

CO2: Analyze the low Voltage effects of devices and judge independently the best suited device for fabrication of smart devices for conducting research in ULSI design.

CO3: Solve problems of Low Voltage design challenges, tradeoff between area, speed and power requirements.

CO4: Apply appropriate techniques, resources and tools to engineering activities in low voltage VLSI circuits.

DETAILED SYLLABUS:

UNIT I: INTRODUCTION TO LOW VOLTAGE DESIGN (Periods:09)
Low-voltage analog circuit design challenges, Design for Low power, Low Power Circuit technologies, Techniques for Leakage Power Reduction, Dynamic Voltage Scaling.

UNIT II: FGMOS, CIRCUIT APPLICATIONS AND DESIGN TECHNIQUES (Periods:09)
The FGMOS Device, Designing with FGMOS, Minimum Input Capacitance, Initial Design ideas, Circuit Applications and design Techniques.

UNIT III: DESIGN FOR LOW POWER (Periods:12)
Lightweight Embedded Systems, Low-Power Design of Systems on Chip, Implementation- Level Impact on Low Power Design, accurate Power

estimation of combinational CMOS digital Circuits, Clock Powered CMOS for Energy-Efficient Computing.

UNIT IV: ANALOG RF CMOS CIRCUITS – I (Periods:12)

Power Considerations – sources of power Dissipation, Limits in Power dissipation, V_{DD} Downscaling, Front-End Challenges, Superheterodyne architecture

UNIT V: ANALOG RF CMOS CIRCUITS – II (Periods:13)

Technology Structural Alternatives, schematic Design Techniques for power saving in RF, RF Amplifier Design, Mixer Design, PLL Design.

Total Periods: 55

TEXT BOOKS:

1. Vojin G.Oklobdzija,"Digital Design and Fabrication", CRC Press, 2nd edition, 2008.
2. Unai Alvarado, Guillermo Bistue and Inigo Adin, "Low Power RF Circuit Design in standard CMOS Technology", Springer, 2011.

REFERENCE BOOKS:

1. Dr Esther Rodriguez-Villegas,"Low Power and Low Voltage Circuit Design with the FGMOS Transistor", the Institution of Engineering and Technology, 2006.
2. Shouri Chatterjee, Kong Pang Pun, et al, "Analog Circuit Design Techniques at 0.5V", Springer, 2007.

M. Tech. (VLSI)-I Semester (Elective-I)
(14MT15709) ULSI TECHNOLOGY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level

COURSE DESCRIPTION:
Cleanroom and wafer-cleaning technology; Fabrication technologies; Device considerations; Assembly, packaging and reliability issues.

COURSE OUTCOMES:
On successful completion of the course the students will be able to
CO1: Demonstrate basic knowledge in ULSI Technology.
CO2: Analyze complex engineering problems critically for conducting research in ULSI Devices.
CO3: Solve engineering problems with wide range of solutions in ULSI.

DETAILED SYLLABUS

UNIT –I: (Periods:10)

Cleanroom technology- Introduction, cleanroom classification, cleanroom design concept, cleanroom installation, cleanroom operation, automation, related facility systems.

Wafer-cleaning technology- Introduction, basic concepts of wafer cleaning, Wet-cleaning technology, Dry-cleaning technology. ULSI Process Technology.

UNIT –II: (Periods:16)

Epitaxy- Introduction, Fundamental Aspects of Epitaxy, Conventional Si Epitaxy, Low temperature Epitaxy of Si, Selective Epitaxial Growth of Si, Characterization of Epitaxial films.

Conventional and Rapid Thermal Processes- Introduction, Requirements for Thermal Processes, Rapid Thermal Processing.

Dielectric and Polysilicon Film Deposition- Introduction, Deposition Processes, APCVD and LPCVD Silicon Oxides, LPCVD Silicon Nitrides, LPCVD Polysilicon Films, Plasma Assisted Depositions, Other Deposition Methods, Applications of Deposited Polysilicon, Silicon Oxide and Silicon Nitride Films.

UNIT –III: (Periods:15)

Lithography- Introduction, Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography.

Etching- Introduction, Low-Pressure Gas Discharge, Etch Mechanisms, Selectivity and Profile Control, Reactive Plasma Etching Techniques and Equipment, Plasma Processing Processes, Diagnostics, End Point Control and Damage, Wet Chemical Etching. **Metallization**- Metal Deposition Techniques, Silicide Process, CVD Tungsten Plug and Other Plug Processes, Multilevel Metallization, Metallization Reliability.

UNIT-IV: (Periods:06)

Process integration- Introduction, Basic Process Modules and Device Considerations for ULSI, CMOS Technology, Bipolar Technology, BiCMOS Technology, MOS Memory Technology, Process Integration Considerations in ULSI Fabrication Technology.

UNIT–V: (Periods:07)

Assembly and Packaging-Introduction, package types, ULSI Assembly Technologies, Package Fabrication Technologies, Package Design Considerations, Special Package Considerations, Other ULSI Packages.

Reliability- Introduction, Hot Carrier Injection, Electromigration, Stress Migration, Oxide Breakdown, Effect of Scaling on Device Reliability, Relations between DC and AC Lifetimes, Some Recent ULSI Reliability Concerns, Mathematics of Failure Distribution.

Total periods: 58

TEXT BOOKS:

1. C.Y.Chang, S.M.Sze,ULSI Technology, McGraw-Hill,2000.
2. Chih-Hang Tung, George T.T.Sheng, Chih-Yuan Lu, ULSI Semiconductor Process Technology Atlas, John Wiley & Sons, 2003.

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M. Tech. – I Semester
(14MT10310) RESEARCH METHODOLOGY
(Common to all M. Tech. Programmes)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	--	--	3

PRE-REQUISITES: --

COURSE DESCRIPTION:

Fundamentals of research work - research problem and design; Data collection, Analysis and hypothesis; Statistics in Research; Interpretation and Report Writing.

COURSE OUTCOMES:

On successful completion of course, the student will be able to

CO1. Demonstrate knowledge on research approaches, research process and data collection.

CO2. Identify and analyze research problem.

CO3. Solve the research problems using statistical methods.

CO4. Carryout literature survey and apply good research methodologies for the development of scientific/ technological knowledge in one or more domains of engineering.

CO5. Learn, select and apply modern engineering tools to complex engineering activities.

CO6. Write effective research reports.

DETAILED SYLLABUS:

UNIT-I: INTRODUCTION TO RESEARCH METHODOLOGY (Periods:07)

Objectives and Motivation of Research, Types of Research, Research Approaches, Research Process, Criteria of good Research.

UNIT-II: RESEARCH PROBLEM AND DESIGN (Periods:09)

Defining and Formulating the Research Problem, Problem Selection, Necessity of Defining the Problem, Techniques involved in Defining a Problem. Features of Good Design, Research Design Concepts, Different Research Designs.

UNIT-III: DATA COLLECTION, ANALYSIS, AND HYPOTHESIS (Periods:09)

Different Methods of Data Collection, Processing Operations, Types of Analysis, Basic Concepts of Testing of Hypothesis, Hypothesis Testing Procedure.

UNIT-IV: STATISTICS IN RESEARCH (Periods:09)

Review of Statistical Techniques - Mean, Median, Mode, Geometric and Harmonic Mean, Standard Deviation, Measure of Asymmetry. Normal Distribution, Chi-Square Test as a Test of Goodness of Fit.

UNIT-V: INTERPRETATION AND REPORT WRITING (Periods:06)

Interpretation – Techniques and Precautions. Report Writing – Significance, Stages, Layout. Types of reports, Precautions in Writing Reports.

Total Periods: 40

TEXT BOOK:

1. C.R. Kothari, *Research Methodology: Methods and Techniques*, New Age International Publishers, New Delhi, 2nd Revised Edition, 2004.

REFERENCE BOOKS:

1. Ranjit Kumar, *Research Methodology: A step-by-step guide for beginners*, Sage South Asia, 3rd ed., 2011.
2. R. Panneerselvam, Research Methodology, PHI learning Pvt. Ltd., 2009

M. Tech. (VLSI)-I Semester
(14MT15721) ANALOG AND DIGITAL IC DESIGN LABORATORY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
25	50	75			4	2

PRE-REQUISITES:

A Course on Digital IC Design and Applications at UG Level.

COURSE DESCRIPTION:
Simulation, synthesis and implementation of digital circuits using HDLs; Modeling and simulation of analog circuits using SPICE.

COURSE OUTCOMES:
On successful completion of the course the students will be able to

CO1: Demonstrate skills in
- SPICE Coding and verification of analog circuits.
- Behavioral system modeling: concurrency and event-driven simulation.
- Digital design modeling using various styles (behavioral, structural and dataflow)
- Designing Combinational and sequential circuits
- Verifying the Functionality of Designed circuits using function Simulator
- Checking for critical path time calculation
- Placement and routing in FPGA
- Implement digital designs on FPGA device for conducting research in the field of Digital Circuits.

CO2: Conceptualize and solve problems in logic verification and timing calculation of Digital circuits.

CO3: Acquire research skills in the domain of Digital Systems.

CO4: Create, develop and use modern CAD tools to analyze problems of RTL, Technology schematic, and system implementation.

CO5: Contribute positively to multidisciplinary scientific research in design and development of Integrated Circuits suited for wide range of applications.

CO6: Perform experiments efficiently in Digital system design to achieve optimization for high device utilization and performance in industrial needs.

DETAILED SYLLABUS:
Modeling and simulation of Analog Circuits using SPICE

1. **Part – I:** **(4 slots)**
   Design and verification of Current Mirror Circuits, Differential Amplifiers, Internal Circuit of OP-AMP, Switched Capacitor Integrator.

Modeling and Functional Simulation of the following digital circuits (with XilinX tools) using VHDL/Verilog Hardware Description Languages

2. **Part-II:** **(4 slots)**
Combinational Logic - Logic Gates, Adders, Encoders, decoders, Multiplexer, Demultiplexer, Comparator, Multipliers, ALU, MAC.

3. **Part – III:** **(4 slots)**
Sequential Logic – Flip-Flops, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial). Memories and State Machines - Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Instruction Fetch, Instruction Decode.

4. **Part-IV:** **(2 slots)**
FPGA System Design - Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation on FPGA/CPLD.

Total Slots: 14

REQUIRED SOFTWARE TOOL:

1. Xilinx10.1 ISE and Above for FPGA/CPLDs.

REFERENCE BOOKS:

1. John F. Wakerly, "Digital Design: Principles and Practices", Prentice Hall, Third Edition, 2000.
2. Analog and Digital Design Lab manual.

M. Tech. (VLSI)-II Semester
(14MT25701) PHYSICAL DESIGN AUTOMATION

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on VLSI Design and Digital IC Design at UG Level

COURSE DESCRIPTION:
Basics of VLSI design; Layout optimization; Simulation and synthesis; Physical design of FPGAs and MCMs.

COURSE OUTCOMES:
On successful completion of the course the students will be able to

CO1. Demonstrate advanced knowledge in
- Algorithmic graph theory
- Tractable and Intractable problems
- Layout compaction such as floor planning, placement and routing
- Binary-Decision diagrams
- Simulation and Synthesis in High level abstraction
- FPGA and MCM technologies

CO2. Analyze complex engineering problems critically in the domain of High-level Synthesis for conducting research.

CO3. Formulate feasible and optimal solutions to solve engineering problems in VLSI Design automation.

CO4. Use EDA tools to apply appropriate algorithms for effective physical design automation.

DETAILED SYLLABUS:

UNIT-I: INTRODUCTION TO VLSI DESIGN METHODOLOGIES (Periods:10)

Introduction to VLSI Design automation tools, Introduction to algorithmic graph theory, Computational Complexity, Tractable and Intractable problems, Combinational optimization.

UNIT-II: LAYOUT COMPACTION (Periods:12)

Design rules, problem formulation, algorithms for constraint graph compaction, placement & partitioning algorithms. Floor planning concepts- shape functions and floor plan sizing, types of routing problems

UNIT -III: SIMULATION AND SYNTHESIS (Periods:10)

Gate Level Modeling and Simulation, Switch Level Modeling and Simulation Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT -IV: HIGH LEVEL SYNTHESIS (Periods:10)

Hardware modeling, internal representation of the input algorithm, allocation, assignment and scheduling algorithms, ASAP scheduling, Mobility based scheduling, list scheduling & force-directed scheduling.

UNIT -V: PHYSICAL DESIGN AUTOMATION OF FPGAs & MCMs (Periods:12)

FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models, MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Routing and Programmable MCMs.

Total periods: 54

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons Pvt. Ltd, 2nd Edition 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", Springer International Edition, 3rd edition, 2005.

REFERENCE BOOKS:

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", John wiley & Sons Pvt. Ltd, 4th edition, 1993.
2. Wayne Wolf, "Modern VLSI Design Systems on silicon", Pearson Education Asia, 2nd Edition, 1998.

M. Tech. (VLSI) - II Semester
(14MT25702) LOW POWER VLSI DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level

COURSE DESCRIPTION:
Concepts of low power design; CMOS and Bi-CMOS processes; Device behavior and modeling; Design of low voltage and low power digital circuits; Special techniques for low power design.

COURSE OUTCOMES:
On successful completion of the course the students will be able to

CO1: Demonstrate in-depth knowledge in
- Limitations of Low Power Design.
- SOI Technology.
- BiCMOS Processes.
- MOSFET and BJT Behavior and Modeling.
- BiCMOS Logic Gates Design.
- Special low power techniques.

CO2: Analyze the low power BiCMOS circuits, the effects of devices and judge independently the best suited device for fabrication of smart devices for conducting research in ULSI design.

CO3: Solve problems of Low power design challenges, tradeoff between area, speed and power requirements.

CO4: Apply appropriate techniques, resources and tools to engineering activities in low power VLSI circuits.

DETAILED SYLLABUS:

UNIT –I **(Periods:12)**

Low Power Design, an Over View: introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS Processes: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT –II: LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES **(Periods:09)**

Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT-III: DEVICE BEHAVIOR AND MODELING **(Periods:11)**

Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT-IV **(Periods:11)**

CMOS and Bi-CMOS Logic Gates: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation

Low-Voltage Low-Power Logic Circuits: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT-V **(Periods:11)**

Low Power Latches and Flip Flops: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

Special Techniques: Power Reduction in Clock Networks, CMOS Floating Node,Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Total Periods: 54

TEXT BOOKS:

1. Yeo Rofail/ Gohl (3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia 1st Indian reprint, 2002.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCE BOOKS:

1. Douglas A.Pucknell & Kamran Eshraghian, "Basic VLSI Design", PHI, 3rd edition.
2. J.Rabaey, "Digital Integrated circuits", PH, 1996.

M. Tech. (VLSI)-II Semester
(14MT25703) MIXED SIGNAL DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Analog Design at UG Level

COURSE DESCRIPTION:
Switched capacitor circuits - analysis and application; Design and characterization of Phase locked loops; Data converters – types and design for different sampling rates.

This course deals with Mixed Signal circuits like Switched Capacitors, PLL, Data Converters, etc. It also deals with design and analysis of Biquad Filters, A/D and D/A converters for different sampling rates.

COURSE OUTCOMES:
On successful completion of the course the students will be able to
CO1: Demonstrate in-depth knowledge in
- Switched Capacitor Circuits
- PLL
- Data Converters – ADC and DAC

CO2: Analyze complex engineering problems critically for conducting research in Data Converters for Communication Systems.
CO3: Solve engineering problems with wide range of solutions to increase Data Rate of ADC and DAC.
CO4:Apply appropriate techniques, resources and tools to engineering activities in development of Data Converters.
CO5: Contribute positively to multidisciplinary scientific research in design and development of Mixed Integrated Circuits suited for wide range of applications.

DETAILED SYLLABUS:
UNIT -I: SWITCHED CAPACITOR CIRCUITS (Periods:14)
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, Biquad filters.

UNIT -II: PHASED LOCK LOOP (PLL) (Periods:08)
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT -III: DATA CONVERTER FUNDAMENTALS (Periods:12)

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based Converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT -IV: NYQUIST RATE A/D CONVERTERS (Periods:08)

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D Converters, Folding A/D converters, Pipelined A/D converters, Time-Interleaved Converters.

UNIT -V: OVERSAMPLING CONVERTERS (Periods:09)

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

Total Periods: 51

TEXT BOOKS:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH Edition, 2002.
2. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, International 2nd Edition/Indian Edition, 2010.
3. David A. Johns,Ken Martin, "Analog Integrated Circuit Design", Wiley Student Edition, 2013.

REFERENCE BOOKS:

1. Rudy Van De Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog converters", Kluwer Academic Publishers, 2003
2. Richard Schreier, "Understanding Delta-Sigma Data converters", Wiley Interscience, 2005.
3. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", Wiley Interscience, 2009.

M. Tech. (VLSI)-II Semester
(14MT25704) RF IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Analog IC Design at UG Level/PG Level

COURSE DESCRIPTION:
Concepts of RF circuits; Transceiver architectures; Low noise amplifier and mixers; Oscillators; Phased locked loop and power amplifier.

COURSE OUTCOMES:
On successful completion of the course the students will be able to
CO1: Demonstrate in-depth knowledge in Radio Frequency Integrated Circuits.
CO2: Analyze complex engineering problems critically for conducting research in RF systems.
CO3: Solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
CO4: Apply appropriate techniques to engineering activities in the field of RFIC Design.

DETAILED SYLLABUS

UNIT – I: BASIC CONCEPTS IN RF DESIGN (Periods:07)
Introduction to RF Design, Units in RF design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

UNIT – II: TRANSCEIVER ARCHITECTURES (Periods:14)
General considerations, Receiver Architectures-Basic Heterodyne receivers, Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers, Low-IF receivers. Transmitter Architectures-Direct Conversion transmitters, Modern direct conversion Transmitters, Heterodyne Transmitters, Other Transmitter Architectures.

UNIT -III: LNA AND MIXERS (Periods:11)
General considerations, Problem of input matching, Low Noise Amplifiers design in various topologies, Gain Switching, Band Switching, Mixers-General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversion mixers.

UNIT – IV: OSCILLATORS (Periods:10)
Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, LC VCOs with wide tuning range, phase noise, Mathematical model of VCOS,Quadrature Oscillators.

UNIT – V: PLL AND POWER AMPLIFIER (Periods:13)

PLLS-Phase detector, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase noise in PLLs, Loop Bandwidth. Power Amplifiers-General considerations, Classification of power amplifiers, High- Efficiency power amplifiers, Cascode output stages, Large signal impedance matching, Linearization techniques.

Total periods: 55

TEXT BOOKS:

1. B.Razavi, "RF Microelectronics", Prentice-Hall PTR, 2nd Edition, 1998.

REFERENCE BOOKS:

1. T.H.Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd, 1998.
2. R.Jacob Baker, Harry W.Li, D.E. Boyce, "CMOS Circuit Design, Layout and Simulation", Prentice-Hall of India, 1998.

M. Tech. (VLSI)-II Semester
(14MT25705) TESTING AND TESTABILITY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:

A Course on Digital Logic Design at UG Level

COURSE DESCRIPTION:
Design for testability; Fault modeling and simulation; Test analysis for digital circuits; Design strategies for testability.

COURSE OUTCOMES:
On successful completion of this course the students will be able to

CO1: Demonstrate advanced knowledge in
- The basic faults that occur in digital systems
- Testing of stuck at faults for digital circuits
- Design for testability

CO2: Analyze testing issues in the field of digital system design critically for conducting research.

CO3: Solve engineering problems by modeling different faults for fault free simulation in digital circuits.

CO4: Apply appropriate research methodologies and techniques to develop new testing strategies for digital and mixed signal circuits and systems.

DETAILED SYLLABUS:

UNIT – I: INTRODUTION TO TEST AND DESIGN FOR TESTABILITY (Periods:13)
Modeling- Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT – II: FAULT MODELLING (Periods:09)
Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, The Single Stuck-Fault Model, The Multiple Stuck-Fault Model.

UNIT-III: FAULT SIMULATION (Periods:07)
Applications, General Fault Simulation Techniques, Fault Simulation for Combinational Circuits, Fault Sampling.

UNIT -IV: TESTING FOR SINGLE STUCK FAULTS (Periods:12)
ATG for SSSFs in Combinational Circuits and Sequential Circuits, Testing for bridging faults, Functional Testing With Specific Fault Models, Vector

Simulation- ATPG Vectors, Formats Compaction and Compression, Selecting ATPG Tool.

UNIT – V: DESIGN FOR TESTABILITY (Periods:11)

Testability Trade Offs, Techniques, Scan Architectures and Testing, Controllability and Observability by means of Scan Registers, Generic Scan-Based Designs, Full Serial Integrated Scan, Storage Cells for Scan Designs, Board-Level and System-Level DFT Approaches, Boundary Scans Standards, Compression Techniques, Different Techniques, Syndrome Testing and Signature Analysis.

Total periods: 52

TEXT BOOKS:

1. MironAbramovici, Melvin A. Breur, Arthur D.Friedman, *"Digital Systems Testing and Testable Design"*, Jaico Publishing House, First edition, 2001.
2. Alfred Crouch, *"Design for Test for Digital ICs & Embedded Core Systems"*, Prentice Hall, First edition, 1999.

REFERENCE BOOKS:

1. Robert J.Feugate, Jr., Steven M.Mentyn, *"Introduction to VLSI Testing"*, Prentice Hall, 1998.

M. Tech. (VLSI)-II Semester (Elective-II)
(14MT25706) ASIC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level

COURSE DESCRIPTION:
ASIC design categories; Design issues, characteristics, design techniques, synthesis, testing and physical design flow of ASIC.

COURSE OUTCOMES:
On successful completion of this course the students will be able to
CO1: Demonstrate in-depth knowledge in
- ASIC Design Styles.
- ASICs Design Issues.
- ASICs Design Techniques.
- ASIC Construction.

CO2: Analyze the characteristics and Performance of ASICs and judge independently the best suited device for fabrication of smart devices for conducting research in ASIC design.
CO3: Solve problems of Design issues, simulation and Testing of ASICs.
CO4: Apply appropriate techniques, resources and tools to engineering activities for appropriate Solution to develop ASICs.

DETAILED SYLLABUS:

UNIT-I **(Periods:11)**

ASIC DESIGN STYLES: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

ASICS– PROGRAMMABLE LOGIC DEVICES: Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Introduction, selected families – design outline.

UNIT-II **(Periods:11)**

ASICS –DESIGN ISSUES: Design methodologies and design tools – design for testability – economies.

ASICS CHARACTERISTICS AND PERFORMANCE: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT-III: ASICS-DESIGN TECHNIQUES **(Periods:08)**

Overview- Design flow and methodology- Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA.

UNIT-IV **(Periods:13)**

LOGIC SYNTHESIS, SIMULATION AND TESTING: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test-fault simulation- automatic test pattern generation.

ASIC CONSTRUCTION: Floor planning, placement and routing system partition.

UNIT-V: FPGA PARTITIONING (Periods:10)

Partitioning Methods-Floor Planning- Placement- Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

Total Periods: 53

TEXT BOOKS:

1. L.J.Herbst, "Integrated circuit engineering", OXFORD SCIENCE Publications, 1996.

REFERENCE BOOKS:

1. M.J.S.Smith, "Application - Specific integrated circuits", Addison-Wesley Longman Inc 1997.

M. Tech. (VLSI)-II Semester (Elective-II)
(14MT25707) CO – DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
Courses on Computer Architecture, Digital Design, Software Design, and Embedded Systems.

COURSE DESCRIPTION:
Co-design issues and algorithms; Prototyping and emulation; Target architectures; Compilation techniques; High level design specification and verification; Language support for co-simulation; Co-design system models – Lycos and Cosyma.

COURSE OUTCOMES: After completion of the course, students should be able to:

CO1. Demonstrate potential knowledge in
- Various design steps starting from system specifications to hardware/software implementation
- Process optimization techniques while considering various design decisions.

CO2. Gain design experience by critically analyzing case studies using contemporary high-level Methods

CO3. Consider trade-offs in the way hardware and software components of a system work together to solve engineering problems to exhibit a specific behavior, given a set of performance goals and technology

CO4. Familiarize with tools to overcome ever increasing embedded system design complexity combined with reduced time-to-market window to revolutionize embedded system design process

DETAILED SYLLABUS

UNIT- I **(Periods:13)**

CO- Design Issues: Co-design Models, Architectures, Languages, a Generic Co-design Methodology

Co-Synthesis Algorithms: Architectural Models, Hardware/Software Partitioning, Distributed System Co-Synthesis

UNIT- II **(Periods:08)**

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping

Target Architectures- I: Architecture Specialization techniques, System Communication infrastructure

UNIT-III: TARGET ARCHITECTURES – II **(Periods:07)**

Target Architecture and Application System classes, Architecture for control dominated systems- 8051. Architectures for High performance control, Architecture for Data dominated systems- ADSP21060, TMS320C. Mixed Systems and Less Specialized Systems

UNIT-IV **(Periods:14)**

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, Practical consideration in a compiler development environment

Design Specification and Verification: Design , co-design, the co-design computational model, concurrency , coordinating concurrent computations, interfacing components, Verification- Design verification and implementation verification, verification tools and interface verification.

UNIT-V **(Periods:13)**

Languages for System- Level Specification and Design: System Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specifications and Multi Language Co-simulation- Concepts for Multi-language design , Co-simulation models.

The Cosyma Systems: Overview, Architecture- design flow and user interaction. Partitioning, Synthesis

Lycos System: Introduction, Partitioning and Design Space Exploration

Total Periods: 55

Text Book:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / software co- design Principles and Practice", Springer, 2009.

Reference Book:

1. Felice Balarine, "Hardware-Software Co-Design of Embedded Systems: The Polis Approach", Springer, 1991.

M. Tech. (VLSI)-II Semester (Elective-II)
(14MT25708) DSP PROCESSORS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Digital Signal Processing at UG Level

COURSE DESCRIPTION:
Principles of digital signal processing; Digital signal processors - architectures and capabilities; Programmable DSPs; Analog families of DSPs; Interfacing of external devices.

COURSE OUTCOMES:
On successful completion of this course the students will be able to
CO1: Demonstrate in-depth knowledge in
- Architectures of Programmable DSP Devices
- Analog Device Families
- Interfacing Memory and I/O Peripherals to Programmable DSP Devices.

CO2: Analyze complex engineering problems critically for conducting research in DSP Processors.
CO3: Solve engineering problems with wide range of solutions in Digital Signal Processing.
CO4: Apply appropriate techniques, resources and tools to engineering activities in Digital Signal Processing.

DETAILED SYLLABUS:
UNIT –I: INTRODUCTION TO DIGITAL SIGNAL PROCESSING **(Periods:15)**
Introduction, A Digital signal processing system, the sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.
Computational Accuracy in DSP Implementations - Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.
UNIT –II: ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES **(Periods:08)**
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III: PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

(Periods:10)

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSP Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV: ANALOG DEVICES FAMILY OF DSP DEVICES (Periods:11)

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Blackfin Processor - The Blackfin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V: INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES (Periods:07)

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

Total Periods: 51

TEXT BOOKS:

1. Avtar Singh and S. Srinivasan, "Digital Signal Processing", Thomson Publications, 2004.
2. K Padmanabhan, R.Vijayarajeswaran, Ananthi. S, "A Practical Approach To Digital Signal Processing", New Age International, 2006/2009.
3. Woon-Seng Gan, Sen M. Kuo, "Embedded Signal Processing with the Micro Signal Architecture", Wiley-IEEE Press, 2007.

REFERENCE BOOKS:

1. B. Venkataramani and M. Bhaskar, "Digital Signal Processors, Architecture, Programming and Applications", TMH, 2002.
2. Jonatham Stein, "Digital Signal Processing" , John Wiley, 2005.
3. Lapsley et al, "DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000.

M. Tech. (CMS & VLSI)-II Semester (Elective-II)
(14MT25709) WIRELESS SENSOR NETWORKS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Wireless Communications at UG Level

COURSE DESCRIPTION:
Concepts of wireless sensor networks; Physical, Network, Transport and Application layers.

COURSE OUTCOMES:
On successful completion of this course the students will be able to

CO1. Demonstrate advanced knowledge in
- Wireless Sensor Networks
- Physical layer
- Data link layer
- Network layer
- Transport layer

CO2. Analyze and design complex problems critically in the domains of Wireless Communications and Wireless sensor Networks for conducting research.

CO3. Apply appropriate techniques to for the development of scientific knowledge in Wireless Sensor Networks.

CO4. Demonstrate knowledge and understanding of wireless sensor networks and apply the same in practice.

DETAILED SYLLABUS

UNIT – I: INTRODUCTION TO WIRELESS SENSOR NETWORKS **(Periods:11)**

Challenges for wireless sensor networks, Comparison of sensor network with ad hoc network, Single node architecture - Hardware components, energy consumption of sensor nodes. Network architecture: Sensor network scenarios- types of sources and sinks, single hop versus multi-hop networks, multiple sinks and sources. Design principles for wireless sensor networks.

UNIT – II: PHYSICAL LAYER **(Periods:11)**

Introduction, wireless channel and communication fundamentals – frequency allocation, modulation and demodulation, wave propagation effects and noise, channels models, spread spectrum communication, packet transmission and synchronization, quality of wireless channels and measures for improvement. Physical layer and transceiver design consideration in wireless sensor networks-Energy usage profile, choice of modulation, Power Management.

UNIT -III: DATA LINK LAYER **(Periods:16)**

MAC protocols: fundamentals of wireless MAC protocols - Requirements and design constraints for wireless MAC protocols, Important classes of MAC

protocols, MAC protocols for wireless sensor networks. Low duty cycle protocols and wakeup concepts - Sparse topology and energy management (STEM), S-MAC, Wakeup radio concepts. Contention-based protocols - CSMA protocols, PAMAS. Schedule-based protocols - SMAC, BMAC, Traffic-adaptive medium access protocol (TRAMA). Link Layer protocols – fundamentals task and requirements, error control - Causes and characteristics of transmission errors, ARQ techniques, FEC techniques, Hybrid schemes, Power control,

UNIT – IV: NETWORK LAYER (Periods:10)

Gossiping and agent-based uni-cast forwarding - Basic idea, Randomized forwarding. Energy-efficient unicast, Broadcast and multicast - Source-based tree protocols, Shared, core-based tree protocols, Mesh-based protocols. geographic routing - Basics of position-based routing, Geocasting. Mobile nodes - Mobile sinks, Mobile data collectors, Mobile regions. Data centric and content-based networking - Introduction, Data-centric routing, Data aggregation.

UNIT – V: TRANSPORT LAYER (Periods:09)

The transport layer and QoS in wireless sensor networks - Quality of service/reliability, Transport protocols. Coverage and deployment - Sensing models, Coverage measures, Uniform random deployments: Poisson point processes, Coverage of random deployments: Boolean sensing model, general sensing model, Coverage determination, Coverage of grid deployments. Reliable data transport, Single packet delivery - Using a single path, Multiple paths, Multiple receivers. Congestion control and rate control - Congestion situations in sensor networks, Mechanisms for congestion detection and handling, Protocols with rate control, The CODA congestion-control framework.

Total periods: 57

TEXT BOOKS:

1. Holger Karl, Andreas willig "Protocol and Architecture for Wireless Sensor Networks", John wiley publication, Oct 2007.

REFERENCE BOOKS:

1. Feng zhao, Leonidas guibas, Elsivier , "Wireless Sensor Networks: an information processing approach –publication, 2004.
2. Edgar H .Callaway, First Edition,"Wireless Sensor Networks : Architecture and protocol", CRC press 2003.
3. C.S.Raghavendra Krishna, M.Sivalingam and Tarib znati, "Wireless Sensor Networks", Springer publication, 2006.

M.Tech (VLSI) – II Semester
(14MT25721) MIXED SIGNAL LABORATORY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
25	50	75	-	-	4	2

PREREQUISITE:
A course on Circuit Level Design and Layouts

COURSE DESCRIPTION:
Design and verification of analog and mixed signal circuits.

COURSE OUTCOMES:
After the completion of the course, the student will be able to

CO1: Discriminate HDL Languages to model FPGA/ASIC design.

CO2: Conceptualize and solve problems in functional verification, timing and Power Analysis of Digital circuits.

CO3: Develop Skills to solve problems of layout design and build solutions for optimizing design for area, power and speed.

CO4: Conduct experiments for modeling devices suited for various communications.

CO5: Able to use CAD Tools to arrive at a optimized solution for mixed signal design.

CO6: Contribute positively to multidisciplinary scientific research in design and development of Mixed/Analog Integrated Circuits to solve problems arising in Integrated circuit Technology.

CO7: Perform projects efficiently in Digital system design to achieve optimization for high device utilization and performance in industrial needs.

DETAILED SYLLABUS:

Mentor Graphic tools / Cadence tools / Synopsis tools

1. **Backend Design** **(8 Slots)**

   Schematic Entry, Simulation, Layout, DRC, PEX, Post Layout Simulation of CMOS Logic Gates, Combinational Circuits (Adders, Encoders, Decoders, Multiplexers, Demultiplexers, etc), Sequential Circuits(Flip Flops, Registers, counters), Biquad Filter, PLL and ADC/DAC.

2. Frontend/Semicustom Design (4 Slots)

HDL Design Entry, Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing
Simulation, Place & Route, Design for Testability, Static Timing Analysis, Power
Analysis of Combinational and Sequential Circuits (Application Oriented designs – Traffic Light Controller, FSM based Control applications, etc).

Total Slots: 12

Required Software Tools:

1. Mentor Graphic tools / Cadence tools / Synopsis tools. (220 nm Technology and Above)
2. Xilinx ISE 10.1i and Above for FPGA/CPLDS.

REFERENCE BOOKS:

1. Mixed Signal Laboratory Manual

M. Tech. (VLSI) – II Semester
(14MT25722) SEMINAR

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
--	50	50	--	--	--	2

PRE-REQUISITES: --

COURSE DESCRIPTION:
Identification of seminar topic; Literature survey; Preparation of technical report and Presentation.

COURSE OUTCOMES:
On successful completion of the course, the student will be able to

CO1. Demonstrate capacity to identify an advanced topic for seminar in core and allied areas.

CO2. Extract information pertinent to the topic through literature survey.

CO3. Comprehend extracted information through analysis and synthesis critically.

CO4. Plan, organize, prepare and present effective written and oral technical report on the topic.

CO5. Adapt to independent and reflective learning for sustainable professional growth.

M. Tech. (VLSI) – III & IV Semesters
(14MT35721 & 14MT45721) PROJECT WORK

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
80	120	200	--	--	--	16

PRE-REQUISITES: --

COURSE DESCRIPTION:
Identification of topic for the project work; Literature survey; Collection of preliminary data; Identification of implementation tools and methodologies; Performing critical study and analysis of the topic identified; Time and cost analysis; Implementation of the project work; Writing of thesis and presentation.

COURSE OUTCOMES:

On successful completion of the course, the student will be able to

CO1. Demonstrate capacity to identify an advanced topic for project work in core and allied areas.

CO2. Gather information related to the topic through literature survey.

CO3. Comprehend gathered information through critical analysis and synthesis.

CO4. Solve engineering problems pertinent to the chosen topic for feasible solutions.

CO5. Use the techniques, skills and modern engineering tools necessary for project work.

CO6. Do time and cost analysis on the project.

CO7. Plan, prepare and present effective written and oral technical report on the topic.

CO8. Adapt to independent and reflective learning for sustainable professional growth.