SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, Tirupati

Department of Electronics and Communication Engineering

Supporting Document for 1.1.2

Syllabus Revision carried out in 2019

Program: M.Tech.- VLSI

Regulations : SVEC-19

This document details the following:

1. Courses where syllabus has been changed 20% and more.
2. Course-wise revised syllabus with changes highlighted.

Note: *For SVEC-19 revised syllabus, SVEC-16 (previous syllabus) is the reference.*

List of Courses where syllabus content has been changed (20% and more)

S. No.	Course Code	Name of the course	Percentage of content changed	Page Number in which Details are Highlighted
1.	19MT15706	VLSI Design Verification and Testing	20	3
2.	19MT15707	FPGA Architectures	70	7
3.	19MT15708	Low Power CMOS VLSI Design	100	11
4.	19MT10708	Research Methodology and IPR	40	15
5.	19MT15731	Analog CMOS VLSI Design Lab	70	19
6.	19MT15732	Digital CMOS VLSI Design Lab	60	23
7.	19MT1AC01	Technical Report Writing	100	27
8.	19MT25701	Nano Materials and Nanotechnology	90	29
9.	19MT25704	Memory Technologies	100	33
10.	19MT25706	Communication Buses and Interfaces	100	35
11.	19MT25707	Network-on-Chip Design	100	37
12.	19MT25731	Physical Design Automation Lab	100	39
13.	19MT2AC01	Statistics with R	100	41
		Average %**(A)**	80.77	
		Total No. of Courses in the Program **(T)**	28	
		No. of Courses where syllabus (more than 20% content) has been changed **(N)**	13	-
		Percentage of syllabus content change in the courses **(C)=(A x N)/100**	10.5	
		Percentage of Syllabus Content changed in the Program (P)= C/T	**37.5**	

DEAN (Academics)
DEAN (Academic)
SREE VIDYANIKETHAN ENGINEERING COLLEGE
Sree Sainath Nagar, A. RANGAMPET
CHITTOOR (DT.)-517 102, A.P.

PRINCIPAL
PRINCIPAL
SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. RANGAMPET
Chittoor (Dist.) - 517 102, A.P., INDIA.

M. Tech. - I/II Semester
(19MT15706) VLSI DESIGN VERIFICATION AND TESTING
(Program Elecive-1)
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Courses on VLSI Design, Digital IC Applications at UG Level.

COURSE OBJECTIVES:

CEO1: To impart in-depth knowledge in generation of test vectors for digital systems.
CEO2: To analyze and test the various faults in digital system design and develop fault free applications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze Modeling of Digital Circuits at various levels of abstraction and various types of logic Simulations.
CO2. Understand the various fault models, reduction techniques to apply for fault sampling and simulation.
CO3. Apply the automatic test generation techniques for testing Single Stuck at Faults and bridging faults in digital circuits.
CO4. Analyze the various testing approaches and Built-In Self Test architectures for testing digital circuits.

DETAILED SYLLABUS:

Unit –I: Introduction to Testing (Hours: 08)
Modeling-Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

Unit–II: Fault Modeling and Simulation (Hours: 09)
Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, Fault Simulation Techniques, Fault Sampling.

Unit-III: Testing for Stuck Faults (Hours: 09)
ATG for SSFs in Combinational Circuits and Sequential Circuits, Detection of Non feedback and Feedback Bridging Faults.

Unit–IV: Design for Testability (Hours: 09)
Controllability and Observability, Scan-Based Designs and Architecture, Board-Level and System-Level DFT Approaches, Compression Techniques, Syndrome Testing and Signature Analysis.

Unit-V: Built-In Self Test **(Hours: 10)**

Introduction to BIST Concepts, Test - Pattern Generation, off-line BIST Architectures, Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO.

Total Hours: 45

TEXT BOOK:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, *"Digital Systems Testing and Testable Design",* Wiley, 1st Edition, 1994.

REFERENCE BOOKS:

1. Alfred L. Crouch, "*Design for Test for Digital ICs & Embedded Core Systems",* Prentice Hall PTR, 1st Reprint Edition, 1999.
2. Robert J.Feugate, Jr., Steven M.McIntyre, "*Introduction to VLSI Testing*", Prentice Hall, 1st Illustrated Edition, 1998.

ADDITIONAL LEARNING RESOURCES

http://www2.eng.cam.ac.uk/~dmh/4b7/resource/section16.htm

https://nptel.ac.in/courses/106103016/21

https://nptel.ac.in/courses/106105161/54

M. Tech. - II Semester
(16MT25705) TESTING AND TESTABILITY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:
A Course on Digital Logic Design at UG Level.

COURSE DESCRIPTION:
Design for testability; Fault modeling and simulation; Test analysis for digital circuits; Design strategies for testability.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - The basic faults that occur in digital systems
   - Testing of stuck at faults for digital circuits
   - Design for testability
2. Analyze testing issues in the field of digital system design critically for Conducting Research.
3. Solve engineering problems by modeling different faults for fault free Simulation in Digital circuits.
4. Apply appropriate research methodologies to develop New testing Strategies for digital and mixed signal circuits and systems.
5. Apply appropriate techniques, Resources and tools in, Modeling to Complex Engineering activities with an understanding of the limitations.
6. Contribute to multidisciplinary scientific work in the field of testing of Stuck at Faults for digital circuits.

DETAILED SYLLABUS:

UNIT –I: INTRODUTION TO TEST AND DESIGN FOR TESTABILITY (Periods: 13)
Modeling-Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT–II: FAULT MODELLING (Periods: 09)
Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, the Single Stuck-Fault Model, The Multiple Stuck-Fault Model.

UNIT-III: FAULT SIMULATION (Periods: 07)
Applications, General Fault Simulation Techniques, Fault Simulation for Combinational Circuits, Fault Sampling.

UNIT-IV: TESTING FOR SINGLE STUCK FAULTS (Periods: 12)
ATG for SSSFs in Combinational Circuits and Sequential Circuits, Testing for bridging faults, Functional Testing With Specific Fault Models, Vector Simulation- ATPG Vectors, Formats Compaction and Compression, Selecting ATPG Tool.

UNIT–V: DESIGN FOR TESTABILITY (Periods: 14)
Testability Trade Offs, Techniques, Scan Architectures and Testing, Controllability and Observability by means of Scan Registers, Generic Scan-Based Designs, Full Serial

Integrated Scan, Storage Cells for Scan Designs, Board-Level and System-Level DFT Approaches, Boundary Scans Standards, Compression Techniques, Different Techniques, Syndrome Testing and Signature Analysis, Introduction to BIST Concepts.

Total periods: 55

TEXT BOOKS:

3. MironAbramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Wiley, 1st Edition, 1994.
4. Alfred L. Crouch, "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall PTR, 1st Reprint Edition, 1999.

REFERENCE BOOK:

1. Robert J.Feugate, Jr., Steven M.Mclntyre, "Introduction to VLSI Testing", Prentice Hall, 1st Illustrated Edition,1998.

M. Tech.– I Semester

(19MT15707) FPGA ARCHITECTURES

(Program Elective-2)

(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Digital Logic Design and VLSI Design at UG Level.

COURSE DESCRIPTION:

Evolution of Programmable Devices, Xilinx, Actel, Altera FPGAs, Logic Synthesis, Technology Mapping, Finite State Machines, Realizations of SM Charts, One Hot Method, System level Design, Device Applications-Fast Bus Controller, FIFO Controller & Intelligent I/O Subsystem

COURSE OBJECTIVES:

CEO1: To impart knowledge in architectures and applications of various families of CPLDs and FPGAs.
CEO2: To develop skills in design, analysis and problem solving for implementation and verification of functions in CPLDs/FPGAs.
CEO3: Apply knowledge and skills for performance analysis in the design of FSMs.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze the architectures of programmable logic devices and technology mapping issues in CPLDs and FPGAs.
CO2. Analyze various Finite state machine charts and its architectures to evaluate the performance of VLSI systems.
CO3. Understand the applications of FPGA in communications, speech processing, Image and video processing.

DETAILED SYLLABUS:

Unit - I: Introduction to Programmable Logic and FPGAs (Hours: 08)

Evolution of Programmable Devices, CPLD Altera Series Max 5000, MAX 7000 Series. Field Programmable Gate Arrays –Design Flow, Placement , Routing Architecture. Altera FPGAs. Advanced Micro Devices (AMD) FPGA. Applications of FPGAs.

Unit - II: (Hours: 09)

Xillinx and Actel FPGAs :

Case Studies – Xilinx XC2000, XilinxXC3000, Xilinx 4000 FPGAS. Actel FPGAs- Actel ACT1, Actel ACT2, Actel ACT3.

Technology Mapping for FPGAs: Logic Synthesis. Lookup Table Technology, Mapping Multiplexer Technology Mapping- The Proserphine Technology Mapper, Multiplexers Technology Mapping in Mis pga, A map and XA map Technology Mappers.

Unit - III: Finite State Machine (Hours: 09)

Finite State Machines, State Transition Table, State Assignment for FPGAs, Hazards and One Hot Encoding. Mustang. State Machine Charts, Derivations of State Machine Charges, Realization of State Machine Charts.

Unit - IV: FSM Architectures and System Level Design (Hours: 10)

Architectures Centered Around Non Registered PLDs, State Machine Designs Centered Around Shift Registers, One – Hot Design Method, Use of ASMs in One Hot Design, Application of One Hot Method. System Level Design – Controller, Data Path and Functional Partition.

Unit - V: Device Applications (Hours: 09)

MAX 5000 Timing, Using Expanders to Build Registered Logic in MAX EPLDs, Simulating Internal Buses in General Purpose EPLDs, Fast Bus Controllers with EPM5016, Micro Channel Bus Master and SDP Logic with the EPM5032 EPLD, FIFO Controller Using an EPM7096, Integrating an Intelligent I/O Subsystem with a Single EPM5130 EPLD.

Total Hours: 45

TEXT BOOKS:

1. S.Brown, R.Francis, J.Rose, Z.Vransic, "*Field Programmable Gate Array*", Kluwer Publication, 1992.
2. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall (PTE), 1994
3. Richard Tinder, "*Engineering Digital Design*", Academic Press, 2nd Edition, 2000.

REFERENCE BOOKS:

1. Charles H. Roth, Jr, "*Fundamentals of Logic Design*", Cengage Learning, 5th Edition, 2004.
2. S.Trimberger, Edr., "*Field Programmable Gate Array Technology*", Kluwer Academic Publications, 1994.

M. Tech. – I Semester
(16MT15707) FPGA ARCHITECTURES & APPLICATIONS
(PE - I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
Fundamentals of Programmable devices; Logic Implementation using PLDs and FPGAs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Demonstrate advanced knowledge in
   - Programmable Logic Devices
   - Different FPGA Architectures
   - Digital Implementation using FPGA
   - FPGA Applications
2. Analyze complex problems critically for digital implementation issues, to conduct research in Digital VLSI Design.
3. Solve engineering problems with wide range of solutions in FPGA Implementation.
4. Initiate research methodologies in Modeling, Simulation and Implementation of complex engineering applications in the field of Digital Design at different levels of abstraction.
5. Apply appropriate techniques, Resources and tools in, Modeling complex engineering applications with an understanding of limitations.
6. Contribute to multidisciplinary scientific work in the field of FPGA Devices.

DETAILED SYLLABUS

UNIT–I: **Programmable logic Devices** **(Periods: 08)**
Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA Features, Architectures and Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT – II: FPGAs **(Periods: 12)**
Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs, Introduction to advanced FPGAs-Xilinx Virtex and ALTERA Stratix

UNIT -III: **(Periods: 14)**
Finite State Machines (FSM): Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.
FSM Architectures: Architectures centered around non registered PLDs, Design of state machines centered around shift registers, One Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.

UNIT – IV: System Level Design: **(Periods: 12)**
Controller, data path designing, Functional partition, Digital front end digital design tools for

FPGAs. System level design using mentor graphics/Xilinx EDA tool (FPGA Advantage/Xilinx ISE), Design flow using FPGAs.

UNIT – V: Case studies **(Periods: 09)**

Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers

Total periods: 55

TEXT BOOKS:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.
2. Richard F. Tinder, "Engineering Digital Design", Academic Press, 2nd edition, 2000.
3. Charles H. Roth, "Fundamentals of logic design", Thomson/Brooks/Cole, 5th edition, 2004.

REFERENCE BOOKS:

1. Pak K. Chan & Samiha Mourad, "Digital Design Using Field Programmable Gate Array", PTR Prentice Hall, 1st edition, 1994.
2. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, "Field Programmable Gate Array", Kluwer Academic Publishers, 1st edition, 1992.

M. Tech. - I Semester
(19MT15708) LOW POWER CMOS VLSI DESIGN
(Program Elective - 2)
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on VLSI Design at UG Level

COURSE DESCRIPTION:

Need for low power VLSI chips, Sources of Power dissipation in MOS & CMOS Devices, Power Estimation, Synthesis of low power VLSI Circuits, Design of low power VLSI Circuits, Low power Memory Architectures, Energy recovery Circuits, Software design of low power VLSI Circuits.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in low power CMOS Circuits.
CEO2: To develop skills in design, analysis and problem solving related to high performance and low power devices.
CEO3: Apply knowledge and skills pertaining to low voltage CMOS circuit design for for wide range of IC applications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze the various power dissipation effects and estimation methods in CMOS VLSI Circuits to improve the performance characteristics of digital systems.
CO2. Understand the various design styles and synthesis of low power and low voltage CMOS VLSI circuits.
CO3. Analyze the various low power Static RAM architectures in design and development of Ultra Low power Integrated Circuits.
CO4. Apply energy recovery techniques to evaluate the performance of low power VLSI Circuits for scientific research in design and development of digital systems.

DETAILED SYLLABUS:

Unit –I **(Hours: 07)**
Power Dissipation in CMOS VLSI design: Need for low power VLSI chips, Sources of Power dissipation, Power dissipation in MOS & CMOS Devices, Limitations of low Power design.

Unit –II **(Hours: 08)**
Power Estimation: Modeling of Signals, Signal Probability Calculation, Probabilistic Techniques for Signal activity Estimation, Statistical Techniques, Estimation of Glitching

Power, Sensitivity Analysis, Power Estimation using input vector Compaction, Estimation of Maximum Power.

Unit-III **(Hours: 10)**

Synthesis for Low Power: Behavioral Level Transforms, Logic Level optimization of low power, Circuit level.

Design and Test of Low Voltage CMOS Circuits: Circuit Design Style, Leakage current in Deep Sub micrometer Transistors, Low voltage Circuit Design Techniques, Multiple Supply Voltages.

Unit-IV **(Hours: 10)**

Low Power Static RAM Architectures: Organization of Static RAM, MOS Static RAM Memory Cell, Banked Organization of SRAMs, Reducing Voltage Swing in Bit lines, Reducing Power in Sense Amplifier Circuits.

Unit-V **(Hours: 10)**

Low Energy Computing using Energy Recovery Techniques: Energy Recovery Circuit Design, Designs with partially Reversible logic, Supply Clock Generation.

Software design for low power: Sources of software power dissipation, software power estimation, Software power estimation, Co-design for low power.

Total Hours: 45

TEXT BOOK:

1. Kaushik Roy, Sharat Prasad, "*Low-Power CMOS VLSI Circuit Design*" Wiley Student Edition, 2000.

REFERENCE BOOK:

1. Kiat-Seng Yeo, Samir S.Rofail and Wang-Ling Goh, "*CMOS/BiCMOS ULSI: Low power, Low Voltage* ", Pearson education, 2002.

M. Tech. – II Semester
(16MT25701) LOW POWER VLSI DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
Low Power Design Limitations; SOI and MOS/BICMOS Processes; Deep submicron processes; Integration/Isolation Considerations; CMOS/Bi-CMOS and Advanced Bi-CMOS Logic Gates; Design and Quality Measures of Low Power Latches & Flip-Flops; Special Low Power Techniques.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
    - Limitations of Low Power Design.
    - SOI Technology.
    - BiCMOS Processes.
    - MOSFET and BJT Behavior and Modeling.
    - BiCMOS Logic Gates Design.
    - Special low power techniques.
1. Analyze the low power BiCMOS circuits, the effects of devices and judge independently the best suited device for fabrication of smart devices for conducting research in ULSI design.
3. Solve problems of Low power design challenges, tradeoff between area, speed and power requirements.
4. Initiate research in low power VLSI design.
5. Apply appropriate techniques, resources and tools to engineering Activities in low power VLSI circuits.
6. Contribute to multidisciplinary scientific work in the field of low power Circuits.

DETAILED SYLLABUS:

UNIT –I: LOW POWER DESIGN AND AN OVER VIEW (Periods: 14)
Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.
MOS/BiCMOS Processes: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT –II: LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES (Periods: 11)
Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT-III: CMOS AND BI-CMOS LOGIC GATES (Periods: 12)
Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.
Low-Voltage Low-Power Logic Circuits: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS.

UNIT-IV: LOW POWER LATCHES AND FLIP FLOPS (Periods: 11)

Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT – V: SPECIAL TECHNIQUES (Periods: 07)

Power Reduction in Clock Networks, CMOS Floating Node,Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Total Periods: 55

TEXT BOOKS:

1. Yeo Rofail/ Gohl (3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia, 1st Indian reprint, 2002.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCE BOOKS:

1. Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design", Prentice Hall, 3rd Illustrated Edition, 1994.
2. J. Rabaey, "Digital Integrated circuits: A Design perspective", Pearson Education, 2nd Edition, 2003.

M. Tech. - I Semester
(19MT10708) RESEARCH METHODOLOGY AND IPR

(Common to all M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	2	-	-	2

PRE REQUISITES:

COURSE DESCRIPTION:

Overview of research; research problem and design; various research designs; Data collection methods; Statistical methods for research;Interpretation& drafting reports and Intellectual property rights.

COURSE OBJECTIVES:

CEO1: To impart knowledge on research methodology and subsequent process involved for successful accomplishment of the research.
CEO2: To impart knowledge on intellectual property rights and subsequent process involved in filing patents and trade mark registration process.
CEO3: To inculcate attitude of reflective learning and contribute to the society through fruitful research.

COURSE OUTCOMES:

On successful completion of the course, students will be able to:

CO1. Apply the conceptual knowledge of research methodology to formulate the hypothesis, data collection and processing, analyzing the data using statistical methods, interpret the observations and communicating the novel findings through a research report.
CO2. Practice ethics and have responsibility towards society throughout the research process and indulge in continuous learning process.
CO3. Apply the conceptual knowledge of intellectual property rights for filing patents and trade mark registration process.

DETAILED SYLLABUS:

Unit-I: Introduction to Research Methodology (Hours: 07)
Objectives and Motivation of Research, Types of Research, Defining and Formulating the Research Problem; Features of research design, Different Research Designs; Different Methods of Data Collection, Data preparation and Processing.

Unit-II: Data Analysis and Hypothesis Testing (Hours: 09)
ANOVA; Principles of least squares-Regression and correlation; Normal Distribution-Properties of Normal Distribution; Testing of Hypothesis – Hypothesis Testing Procedure, Types of errors, t-Distribution, Chi-Square Test as a Test of Goodness of Fit.

Unit-III: Interpretation and Report Writing (Hours: 04)
Interpretation – Need, Techniques and Precautions; Report Writing – Significance, Different Steps, Layout, Types of reports,Mechanics of Writing a Research Report, Precautions in Writing Reports; Research ethics.

Unit-IV: Introduction to Intellectual property and Trade Marks (Hours: 07)
Importance of intellectual property rights; types of intellectual property, international organizations; Purpose and function of trademarks, acquisition of trade mark rights, protectable matter, selecting and evaluating trade mark, trade mark registration processes.

Unit-V: Law of Copyrights (Hours: 08)
Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.
Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer
New Developments in IPR: Administration of Patent System.

Total Hours: 35

TEXT BOOKS:

1. C.R. Kothari, *Research Methodology: Methods and Techniques*, 2nd revised edition, New Age International Publishers, New Delhi, 2004.
2. Deborah, E. Bouchoux, *Intellectual property right*, 5th edition, Cengage learning, 2017.

REFERENCE BOOKS:

1. R. Panneerselvam, *Research Methodology*, PHI learning Pvt. Ltd., 2009.
2. Prabuddha Ganguli, *Intellectual property right - Unleashing the knowledge economy*, Tata McGraw Hill Publishing Company Ltd, 2001.

M. Tech. – I Semester
(16MT13808) RESEARCH METHODOLOGY
(Common to all M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	-	2	-	-

PREREQUISITES: --

COURSE DESCRIPTION:

Overview of Research, research problem and design, various research designs, data collection methods, statistical methods for research, importance of research reports and its types.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Acquire in-depth knowledge on
   - Research design and conducting research
   - Various data collection methods
   - Statistical methods in research
   - Report writing techniques.
2. Analyze various research design issues for conducting research in core or allied areas.
3. Formulate solutions for engineering problems by conducting research effectively in the core or allied areas.
4. Carryout literature survey and apply research methodologies for the development of scientific/technological knowledge in one or more domains of engineering.
5. Select and Apply appropriate techniques and tools to complex engineering activities in their respective fields.
6. Write effective research reports.
7. Develop attitude for lifelong learning to do research.
8. Develop professional code of conduct and ethics of research.

DETAILED SYLLABUS:

Unit-I: Introduction to Research Methodology (Periods: 5)
Objectives and Motivation of Research, Types of Research, Research Approaches, Research Process, Criteria of good Research, Defining and Formulating the Research Problem, Problem Selection, Necessity of Defining the Problem, Techniques involved in Defining a Problem.

Unit-II: Research Problem Design and Data Collection Methods (Periods: 7)
Features of Good Design, Research Design Concepts, Different Research Designs, Different Methods of Data Collection, Data preparation: Processing Operations, Types of Analysis.

Unit-III: Statistics in Research (Periods:6)
Review of Statistical Techniques - Mean, Median, Mode, Geometric and Harmonic Mean, Standard Deviation, Measure of Asymmetry, ANOVA, Regression analysis.

Unit-IV: Hypothesis Testing (Periods: 7)

Normal Distribution, Properties of Normal Distribution, Basic Concepts of Testing of Hypothesis, Hypothesis Testing Procedure, Hypothesis Testing: t-Distribution, Chi-Square Test as a Test of Goodness of Fit.

Unit-V: Interpretation and Report Writing (Periods: 3)

Interpretation – Techniques and Precautions, Report Writing – Significance, Stages, Layout, Types of reports, Precautions in Writing Reports.

Total Periods: 28

TEXT BOOK:

1. C.R. Kothari, "*Research Methodology: Methods and Techniques*," New Age International Publishers, New Delhi, 2nd Revised Edition, 2004.

REFERENCE BOOKS:

1. Ranjit Kumar, "*Research Methodology: A step-by-step guide for beginners*," Sage South Asia, 3rd ed., 2011.
2. R. Panneerselvam, "Research Methodology," PHI learning Pvt. Ltd., 2009

M. Tech. – I Semester
(19MT15731) ANALOG CMOS VLSI DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

A Course on electronic circuit analysis and VLSI Design at UG Level.

COURSE DESCRIPTION:

Single Stage CMOS Amplifiers, Cascode Amplifiers, Feedback Amplifiers, Operational Amplifiers, Gain Boosting and Frequency Compensation Techniques, Bandgap References, Switched Capacitor Circuits, Sampling Switches, Ring Oscillator, PLL.

COURSE OBJECTIVES:

CEO1: To impart knowledge on modeling Analog circuits.
CEO2: To develop and apply techniques for boosting gain and compensating frequency.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Design and Develop Feedback Amplifiers and Operational Amplifiers.
CO2. Apply suitable compensation techniques to design CMOS circuits.
CO3. Analyze various Bandgap references to compensate the issues in design specifications.
CO4. Develop switched capacitor circuits for various filter designs.
CO5. Work individually and in groups to solve problems with effective communication.

List of Exercises /Experiments: (10-12 Exercises/Experiments)

1. Model the single stage amplifiers (Common Source Amplifier, Common Drain Amplifier, Common Gate Amplifier) using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.

2. Model the Differential Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.

3. Model the Cascode Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.

4. Model the Operational amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like gain, Output Resistance, Power Dissipation, etc.

5. Model the Feedback Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like gain, Output Resistance, Power Dissipation, etc.

6. Model and apply the gain boosting techniques to CMOS amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Power Dissipation, etc.

7. Model and apply the frequency compensation techniques to CMOS amplifiers using SPICE Language, develop their schematic and layout to obtain their frequency response.

8. Model Bandgap Reference Circuits by using SPICE Language, develop their schematic and layout to obtain their Characteristics.

9. Model Sampling Switches using SPICE Language, develop their schematic and layout to obtain their characteristics.

10. Model Switched Capacitor Amplifier and Integrator using SPICE Language, develop their schematic and layout to obtain their characteristics.

11. Model Ring Oscillator using SPICE Language, develop their schematic and layout to obtain their characteristics.

12. Model Phase Locked Loop using SPICE Language, develop their schematic and layout to obtain their characteristics.

13. Mini Projects (MPs):
    Form a group of maximum 2 members as a team and assign mini projects related to Development of compensation techniques and design of alternative subsystem designs.

REFERENCE BOOKS/LABORATORY MANUALS

1. ECE Department *Analog CMOS VLSI Design* Lab Manual.
1. Behzad Razavi, "*Design of Analog CMOS Integrated Circuit*", Tata McGraw-Hill, 14th Reprint 2008.

SOFTWARE/TOOLS USED:

Cadence/synopsys/mentor graphics

ADDITIONAL LEARNING RESOURCES

1. https://nptel.ac.in/courses/117101105/

M. Tech. - I Semester
(16MT15731) ANALOG IC DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	--	--	4	2

PRE-REQUISITES:
A Course on Linear IC Applications at UG Level.

COURSE DESCRIPTION:
Modeling and simulation of analog circuits using SPICE.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Demonstrate knowledge in design of analog circuits.
2. Exhibit skills in SPICE Coding and verification of analog circuits.
3. Solve problems in Modeling and analysis of MOSFETs and OPAMPs.
4. Develop Skills to solve problems of design and analysis of analog circuits.
5. Initiate research in analog IC design.
6. Able to use CAD Tools to arrive at an optimized solution for analog signal design.
7. Contribute positively to multidisciplinary scientific research in design and development of Analog Integrated Circuits to solve problems arising in Integrated circuit Technology.
8. Communicate effectively in Verbal and written form of designs developed.

LIST OF EXERCISES:

Modeling and simulation of Analog Circuits using SPICE

1. Study of MOS Characteristics and Characterization.
2. Design and Simulation of single ended and differential Amplifiers.
3. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier).
4. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier).
5. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing).
6. Design and Simulation of Basic Current Mirror, Cascode Current Mirror and Active Current mirrors.
7. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier.
8. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier.
9. Design and Simulation of Switched Capacitor.
10. Design and Simulation of various types of first and second order active filters and its applications.
11. Design and Simulation of full wave precision rectifier using opamp.
12. Design and simulation of basic applications based on opamp.

Total Time Slots: 12

REQUIRED SOFTWARE TOOL:
1. Cadence/Synopsys/Mentor graphics Tools.

REFERENCE BOOKS:

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2001.
2. Ken Martin, Analog Integrated Circuit Design, Wiley Publications, 2002.
3. Analog IC Design Lab manual.

M. Tech. – I Semester
(19MT15732) DIGITAL CMOS VLSI DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

A Course on electronic circuit analysis and VLSI Design at UG Level.

COURSE DESCRIPTION:

Alternate CMOS combinational and sequential Logic Circuits, Clock Generation, Skew and Synchronization, Logical Effort, Memories, Adders, Multipliers, Shifters, ALU, Arithmetic Processor, Pipelining.

COURSE OBJECTIVES:

CEO1: To impart knowledge on modeling Digital CMOS circuits.
CEO2: To develop programming skills to solve problems in designing subsystems or processors.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze CMOS logic styles for combinational and sequential circuits.
CO2. Design and develop alternative subsystems for the design of a processor.
CO3. Design CMOS memories for high speed networks.
CO4. Work individually and in groups to solve problems with effective communication.

List of Exercises/Experiments: (10-12 Exercises/Experiments)

1. Model alternate CMOS Logic styles for Logic Gates using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

2. Model static and dynamic CMOS Logic for sequential circuits using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

3. Model clock generation circuits for synchronization to avoid skew using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

4. Model the effect of Logical Effort on CMOS Logic using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

5. Model SRAM and DRAM using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

6. Model n-bit Adder using Hardware Description Language and perform its functional simulation.

7. Model n-bit Modified Booth Multiplier using Hardware Description Language and

perform its functional simulation.

8. Model n-bit Barrel Shifter using Hardware Description Language and perform its functional simulation.

9. Model n-bit Arithmetic and Logic Unit using Hardware Description Language and perform its functional simulation.

10. Design Read Only Memory (ROM), Random Access Memory (RAM), Model them using Hardware Description Language and perform its functional simulation.

11. Design a 4-bit Arithmetic Processor with and without pipelining, Model it using Hardware Description Language and perform its functional simulation.

12. Implementation of Experiments 6 to 11 on FPGA/ CPLD.

13. Mini Projects (MPs):
Form a group of maximum 2 members as a team and assign mini projects related to Development of compensation techniques and design of alternative subsystem designs.

REFERENCE BOOKS/LABORATORY MANUALS

1. ECE Department Digital CMOS VLSI Design Lab Manual.
2. Jan M Rabaey, "Digital Integrated Circuits", Pearson Education, 2nd Edition, 2003.

SOFTWARE/TOOLS USED:

Cadence/synopsys/mentor graphics/ Xilinx

ADDITIONAL LEARNING RESOURCES

1. https://onlinecourses.nptel.ac.in/noc19_ee25
2. https://nptel.ac.in/courses/117101105/

M. Tech. - I Semester
(16MT15732) DIGITAL IC DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	--	--	4	2

PRE-REQUISITES:
A Course on Digital IC Applications at UG Level.

COURSE DESCRIPTION:
Modeling, Simulation, Synthesis and Implementation of digital circuits using HDLs;

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in design of digital circuits.
2. Exhibit analytical skills in
   - Behavioral system modeling: concurrency and event-driven simulation.
   - Digital design modeling using various styles (behavioral, structural and dataflow)
   - Designing Combinational and sequential circuits
   - Verifying the Functionality of Designed circuits using function Simulator
   - Checking for critical path time calculation
   - Placement and routing in FPGA
   - Implement digital designs on FPGA device for conducting research in the field of Digital Circuits.
3. Conceptualize and Solve problems in logic verification and timing calculation of Digital circuits.
4. Initiate research in digital IC design.
5. Acquire research skills in the domain of Digital Systems.
6. Create, develop and use modern CAD tools to analyze problems of RTL, Technology schematic, and system implementation.
7. Contribute positively to multidisciplinary scientific research in design and development of Digital Integrated Circuits to solve problems arising in Integrated circuit Technology.
8. Communicate effectively in Verbal and written forms for the designs developed.

LIST OF EXERCISES:

Modeling and Functional Simulation of the following digital circuits (with XilinX tools) using Verilog Hardware Description Languages

Part–I: Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Substractor, Multipliers, Decoders, Address decoders, parity generator, ALU

Part–II: Sequential Logic: D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder / Decoder.

Part–III: Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs

Part-IV: FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of Mini-Project on FPGA/CPLD

Total Time Slots: 12

REQUIRED SOFTWARE TOOL:

1. Xilinx10.1 ISE and Above for FPGA.

REFERENCE BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan, & Borivoje Nikolic, "Digital Integrated Circuits – A design perspective", Prentice Hall, 3rd Edition, 2008.
2. Digital IC Design Lab manual.

M. Tech. - I Semester
(19MT1AC01) TECHNICAL REPORT WRITING
(Audit Course)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	*2*	-	-	-

PRE-REQUISITES: -

COURSE DESCRIPTION:

Introduction; Process of writing; Style of writing; Referencing; Presentation.

COURSE OBJECTIVES:

CEO1: To impart the knowledge of structure and layout of Business and Technical Reports.
CEO2: To learn styles and techniques of description for effective reports.
CEO3: To develop the ability to understand & interpret the writing techniques for effective communication in written documents.

COURSE OUTCOMES:

After successful completion of this course, the students will be able to:

CO1. Demonstrate knowledge of Technical Report Writing by examining kinds of reports and structure with scientific attitude.
CO2. Apply the techniques in preparing effective reports by examining Techniques of Description, Describing Machines and Mechanisms and Describing Processes.
CO3. Communicate effectively through writing technical reports by demonstrating the knowledge of Industry Reports, Survey Reports, Interpretive Report and Letter Report.

DETAILED SYLLABUS:

Unit I - **Introduction** **(Hours: 06)**
Introduction to Technical Report - Types of Reports - Planning Technical Report Writing - Components of a Technical Report - Report Writing in Science and Technology - Selecting and Preparing a 'Title' - Language Use in Report Writing.

Unit II - **Process of Writing** **(Hours: 05)**
Writing the 'Introduction' - Writing the 'Materials and Methods' – Writing the Findings/Results'- Writing the 'Discussion' - Preparing and using 'Tables'.

Unit III - **Style of Writing** **(Hours: 06)**
Preparing and using Effective 'Graphs' - Citing and Arranging References—I - Citing and Arranging References —II - Writing for Publication in a Scientific Journal.

Unit IV - **Referencing** **(Hours: 09)**
Literature citations - Introductory remarks on literature citations - Reasons for literature citations – Bibliographical data according to ISO - Citations in the text - Copyright and copyright laws - The text of the Technical Report - Using word processing and desktop publishing (DTP) systems - Document or page layout and hints on editing - Typographic details - Cross-references.

Unit IV - **Presentation** **(Hours: 04)**

Giving the presentation - Appropriate pointing - Dealing with intermediate questions - Review and analysis of the presentation - Rhetoric tips from A to Z.

Total Hours: 30

TEXT BOOKS:

1. R C Sharma – Krishna Mohan, *"Business Correspondence and Report Writing,"* Tata McGraw-Hill Publishing Company Limited, New Delhi, Third Edition, 2005 (reprint).
2. Patrick Forsyth*, "How to Write Reports and Proposals",* THE SUNDAY TIMES (Kogan Page), New Delhi, Revised Second Edition, 2010.

REFERENCE BOOKS:

1. John Seely, "*The Oxford Writing & Speaking"*, Oxford University Press, Indian Edition.
2. Anne Eisenberg, "*A Beginner's Guide to Technical Communication"*, McGraw Hill Education (India) Private Limited, New Delhi, 2013.

ADDITIONAL LEARNING RESOURCES

1. http://www.resumania.com/arcindex.html
2. http://www.aresearchguide.com/writing-a-technical-report.html
3. http://www.sussex.ac.uk/ei/internal/forstudents/engineeringdesign/studyguides/tec report writing

M. Tech. – II Semester
(19MT25701) NANO MATERIALS AND NANOTECHNOLOGY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Basic Engineering Physics, Basic Engineering Chemistry and Electronic Devices at UG Level.

COURSE DESCRIPTION:

Nanostructures – Classification and Peculiarities, Characterization and Properties of Nanomaterials, Micro Electro-Mechanical Systems (MEMS) & Nano Electro-Mechanical Systems (NEMS), Carbon Nanotubes (CNT) – Properties and Synthesis, Interdisciplinary Applications of Nanomaterials.

COURSE OBJECTIVES:

CEO1: To relate unique properties of nanomaterials to the reduce dimensionality of the material.
CEO2: To impart skills on nanostructures fabrication.
CEO3: To provide knowledge on nanomaterials and implication of health and safety related to nanomaterials.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand the peculiarities of Nanostructured materials, their characterization and properties to solve structural, mechanical and electrical problems in manufacturing Nanostructures.
CO2. Use IC Fabrication techniques to manufacture Micro Electro-Mechanical Systems (MEMS) and Nano Electro-Mechanical Systems (NEMS).
CO3. Understand carbon nanotube properties and its synthesis for various applications.
CO4. Apply the properties of nanomaterials by fixing the boundaries in system development in multidisciplinary areas like Automobiles, Biomedical, Agriculture.

DETAILED SYLLABUS:

Unit - I: Nanostructures and Peculiarities of Nanostructured Materials (Hours: 09)

Gleiter's classification of nanostructured materials, Classification of nanostructures by dimensionality, Concept of "surface form engineering" in nanomaterial science, Extended internal surface, Increasing of surface energy and tension, Grain boundaries, Instability of 3D0 NSM due to grain growth.

Unit – II: Characterization and Properties of Nanomaterials (Hours: 11)

Structural Characterization: X-ray diffraction (XRD),Scanning electron microscopy (SEM), Transmission electron microscopy (TEM), Chemical Characterization: Optical spectroscopy, Electron spectroscopy, Ionic spectrometry, Physical Properties of Nanomaterials: Melting points and lattice constants, Mechanical properties, Optical properties Electrical conductivity.

Unit – III: Micro Electro-Mechanical Systems (MEMS) and Nano Electro-Mechanical Systems (NEMS) (Hours: 08)

Introduction, Fabrication of MEMS and NEMS, Surface micromachining, Bulk Micromachining, Fabrication stages, Deposition, Patterning, Etching.

Unit – IV: Carbon Nanotubes (CNT) – Properties and Synthesis (Hours: 09)

Dimensions, Chirality, Material Properties, Mechanical Properties, Electrical Properties, Optical Properties, Thermal Properties, Nanotube Growth Methods, Chemical Vapor Deposition, Thermal Chemical Vapor Deposition, Other Growth Methods: Arc Discharge, Laser Ablation, Applications

Unit – V: Interdisciplinary Arena of Nanomaterials (Hours: 08)

Molecular Electronics and Nanoelectronics, Nanobots, Biological Applications of Nanoparticles, Catalysis by Gold Nanoparticles, Band Gap Engineered Quantum Devices, Nanomechanics Carbon Nanotube Emitters, Photoelectrochemical Cells, Photonic Crystals and Plasmon Waveguides

Total Hours: 45

TEXT BOOKS:

1. A I Gusev and A ARempel, "*Nanocrystalline Materials*", Cambridge International Science Publishing, 1st Indian edition, 2008.
2. Guozhong Cao and Ying Wang, "*Nanostructures and Nanomaterials: Synthesis, Properties, and Applications",* Imperial College Press, 2004.

REFERENCE BOOKS:

1. Bhushan, Bharat, "*Springer Handbook of Nanotechnology*", 2nd edition, 2006.
2. Pokropivny, Vladimir, Rynno Lohmus, Irina Hussainova, Alex Pokropivny, and Sergey Vlassov, "*Introduction to nanomaterials and nanotechnology*", Tartu, Estonia: Tartu University Press, 2007.
3. Kamal K. Kar, *"Carbon Nanotubes: Synthesis, Characterization and Applications",* Research Publishing Services, 1st edition, 2011.

ADDITIONAL LEARNING RESOURCES

1. *Introduction to Nanotechnology,* nanohub.org
2. https://nptel.ac.in/courses/103103033/module9/lecture1.pdf

M.Tech. - II Semester
(16MT25703) NANOELECTRONICS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
Courses on Basic Engineering Physics, Basic Engineering Chemistry and Electronic Devices at UG level.

COUSRE DESCRIPTION:
Introduction to wave particle nature and mechanics; Crystal structure of semiconducting material; Material for nanoelectronics; Different techniques of nanostructure fabrication; Nanostructure Characterization; Electron transport mechanism.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - wave particle nature, wave mechanics,
   - crystal structure of semiconducting material
   - different techniques of nanostructure fabrication,
   - characterization of the nanostructure and electron in well
2. Analyze
   - Crystal structure of nanomaterials
   - Nanostructure based device
3. Design and develop new nanodevices for advanced technological applications.
4. Efficiently solve complex problems in the field of nanoelectronics.
5. Involve and resolve the future research challenges in the fields related to Nanoelectronics.
6. Contribute to multidisciplinary research in biotechnology, MEMS, other nanotechnology fields.

DETAILED SYLLABUS:

UNIT I -PARTICLES AND WAVE MECHANICS (periods: 10)
Introduction classical particles, classical waves, wave–particle duality, Wave mechanics, Schrodinger wave equation, wave mechanics of particles, atoms and atomic orbital's.

UNIT II - MATRIAL FOR NANOELECTRONICS (periods: 10)
Introduction, Semiconductors, Crystal structure and Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor heterostructures, Lattice-matched and pseudomorphic heterostructure, Organic semiconductors, Carbon nanomaterials: nanotubes and fullerenes.

UNIT III - FABRICATION AND CHARACTERISATION OF NANOSTRUCTURES (periods: 12)
Bulk crystal and heterostructure growth, Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices, Characterization techniques of nanostructures, Spontaneous formation and ordering of nanostructures, Nanocrystals and

nanoclusters, Methods of nanotube growth, Chemical and biological methods for nanoscale fabrication, Fabrication of nanoelectromechanical systems.

UNIT IV - ELECTRON TRANSPORT AND TRADITIONAL LOW-DIMENSIONAL STRUCTURES (periods: 10)

Electron Transport In Nanostructures

Introduction, Time and length scales of the electrons in solids, Statistics of the electrons in solids and nanostructures, The density of states of electrons in nanostructures, Electron transport in nanostructures.

Electrons In Traditional Low-Dimensional Structures

Introduction, Electrons in quantum wells, Electrons in quantum wires, Electrons in quantum dots.

UNIT V -NANOELECTRONIC DEVICES (periods: 13)

General Properties, Resonant Tunneling Diode, Operating Principle and Technology, Applications in High Frequency and Digital Electronic, Circuits and Comparison with Competitive Devices, Quantum Cascade Laser, Operating Principle and Structure, Quantum Cascade Lasers in Sensing and Ultrafast Free, Space Communication Applications, Single Electron Transistor, Operating Principle, Technology, Applications, Carbon Nanotube Devices Structure and Technology, Carbon Nanotube Transistors.

Total Periods: 55

TEXT BOOKS:

1. V. Mitin, V. Kochelap, M. Stroscio, "Introduction to Nanoelectronics", Cambridge University Press (2008).
2. W.R.Fahrner, "Nanotechnology and Nanoelectronics – Materials, Devices, Measurement Techniques", Springer-Verlag Berlin, Germany (2005).

REFERENCE BOOKS:

1. Supriyo Datta, "Lessons from Nanoelectronics: A New Perspective on Transport", World Scientific Publishing Co. Pte. Ltd. 5 Toh Tuck Link, Singapore 596224, Vol. 1, (2012).
2. Bhushan, Bharat, "Springer Handbook of Nanotechnology", 2nd edition, 2006.

M. Tech. - II Semester
(19MT25704) MEMORY TECHNOLOGIES
(Program Elective - 3)
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Digital Electronics and VLSI design at UG Level

COURSE DESCRIPTION:

Random access memory Technology; Non-Volatile memory designs; Reliability and Radiation effects of semiconductor memory; Packaging technologies, Fault modeling and Testing of memory.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge on various memory Technologies.
CEO2: To develop skills in design and analysis of different memory architectures and Packaging.
CEO3: Apply knowledge and skills to develop optimized memory design to solve real time problems.

COURSE OUTCOMES:

On successful completion of the course, students will be able to

CO1. Understand various Random Access Memory Technologies, Non-Volatile Memory Designs and Technologies for optimized memory design.
CO2. Analyze the reliability and radiation issues of semiconductor memories for different memory Architectures.
CO3. Apply advanced memory and high packaging technologies in memory optimization.
CO4. Use the various memory fault models and appropriate testing Techniques to improve the performance of systems.

DETAILED SYLLABUS:

Unit – I: Random Access Memory Technologies (Hours: 11)
Static Random Access Memories (SRAMs): Basic SRAM Architecture and Cell Structures, High performance SRAMs, Advanced SRAM Architectures , BiCMOS SRAMs, Low-Voltage SRAMs ,SOI SRAMs, Specialty SRAMs.
Dynamic Random Access Memories (DRAMs): DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs, Cache DRAM, Virtual Channel Memory (VCM) DRAMs, Multilevel Storage DRAMs , SOI DRAMs , Gigabit DRAM Scaling Issues and Architectures, Advanced DRAM design and Architecture, Application Specific DRAMs.

Unit – II: Non-Volatile Memory Designs and Technologies (Hours: 08)
Masked Read-Only Memories (ROMs), Programmable Read-Only Memories (PROMs), Non-volatile memory advances, Floating Gate Cell Theory and Operations, Erasable (UV) -

Programmable Road-Only Memories (EPROMs), Electrically Erasable PROMs (EEPROMs), Flash Memories, Multilevel Nonvolatile Memories.

Unit – III: Semiconductor Memory Reliability and Radiation Effects (Hours: 09)
Reliability: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory Reliability, Reliability Modeling, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification.
Radiation: Radiation Effects, Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics, Radiation hardness assurance.

Unit – IV: Advanced Memory and High-Density Packing Technologies (Hours: 09)
Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto resistive Random Access Memory, Experimental Memory Devices. Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory Cards, High Density Memory Packaging Future Directions.

Unit – V: Memory Fault Modeling and Testing (Hours: 08)
RAM Fault Modeling, Electrical Testing, RAM Peusdo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing, Memory error detection and correction Techniques.

Total Hours: 45

TEXT BOOKS:

1. Ashok K Sharma, *"Advanced Semiconductor Memories: Architectures, Designs and Applications"*, Wiley Interscience, 2003.
2. Ashok K Sharma,"*Semiconductor Memories:Technology*", Testing & Reliability, PHI, 2012.

REFERENCE BOOKS:

1. Kiyoo Itoh, "*VLSI memory chip design*", Springer International Edition, 2001.
2. Luecke Mize Carr, "*Semiconductor Memory design and Application*", Mc-Graw Hill, 1973

ADDITIONAL LEARNING RESOURCES

https://researcher.watson.ibm.com/researcher/view_group.php?id=7956
https://www.electronics-notes.com/articles/electronic_components/semiconductor-ic-memory/memory-types-technologies.php
https://nptel.ac.in/courses/117106111/24
https://nptel.ac.in/courses/106105033/32
https://nptel.ac.in/courses/106104122/30
https://nptel.ac.in/courses/117101058/28

M. Tech. – II Semester
(19MT25706) COMMUNICATION BUSES AND INTERFACES
(Program Elective – 4)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Computer Organization and Microprocessor & Microcontrollers.

COURSE DESCRIPTION:

Serial Busses, RS232 – Limitations and Applications, CAN Protocol, USB – Types, Architecture, Serial Communication Protocol using Physical Medium.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in design of Communication protocols and interfaces.
CEO2: To develop skills in design, analysis and problem solving for high speed data transfer among communication devices.
CEO3: To apply knowledge and skills of physical interconnects and standards for the development of new communication busses and physical interfaces.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand the features of various serial protocols for high speed data communication between ICs in a Board.
CO2. Analyze the limitations of RS232 to solve the problems in various communicating devices.
CO3. Develop the architecture of Controller Area Network for Application layer communication.
CO4. Apply PCIe hardware Protocol for high speed communication between compatible devices.
CO5. Apply appropriate serial communication protocols and USB transfer types for high performance communication bus.

DETAILED SYLLABUS:

Unit – I: Serial Bus (Hours: 06)
Physical interface, Data and Control signals, features

Unit – II: Introduction to Serial standards (Hours: 08)
Limitations and applications of RS232, RS485, I2C, SPI

Unit - III: Controller Area Network (Hours: 10)
CAN - Architecture, Data transmission, Layers, Frame formats, applications

Unit – IV: Introduction To PCIe (Hours: 08)
PCIe - Revisions, Configuration space, Hardware protocols, applications

Unit – V: Universal Serial Bus (Hours: 13)
USB - Transfer types, enumeration, Descriptor types and contents, Device driver.
Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

Total Hours: 45

TEXT BOOKS:

1. Jan Axelson, *"Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems"*, Lakeview Research, 2nd Edition.
2. Marco Di Natale, Haibo Zeng, Paolo Giusto, Arkadeb Ghosal, "*Understanding and Using the Controller Area Network Communication Protocol: Theory and Practice*" Springer Science & Business Media, 2012.

REFERENCE BOOKS:

1. Wilfried Voss, "*A Comprehensible Guide to Controller Area Network*", Copperhill Media Corporation, 2nd Edition, 2005.
2. Jan Axelson, "*USB Complete*", Penram Publications.
3. Mike Jackson, Ravi Budruk, "*PCI Express Technology*", Mindshare Press.

ADDITIONAL LEARNING RESOURCES

https://nptel.ac.in/courses/108102045/17
https://nptel.ac.in/courses/117106111/36
https://nptel.ac.in/courses/117104072/26
https://nptel.ac.in/courses/108107029/65

M. Tech. – II Semester
(19MT25707) NETWORK-ON-CHIP DESIGN
(Program Elective – 4)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on VLSI Design and parallel processing and Computing at UG Level

COURSE DESCRIPTION:

NOC –Architecture Design, Switching Technique ;Routing Algorithm ;Fault tolerance; Testing;3D NOC ;Optical NOC.

COURSE OBJECTIVES:

CEO1: To impart in-depth knowledge in Network on – chip Architecture and fault tolerance.
CEO2: To develop skills in design, analysis, problem solving and research in various routing algorithms.
CEO3: To apply knowledge and skills for development of applications in 3D Network On-chip Design.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand Network on-chip topologies, routing strategies and architectures to improve Quality of Service in communication applications.
CO2. Develop routing algorithms to solve problems of congestion and flow in multicast routing for 2D and 3D Mesh Networks.
CO3. Apply Security and Monitoring Services to reduce the occurrence of dead and Live lock condition during data transmission and Fault tolerance.
CO4. Analyze three-Dimensional Integration of Network-On-Chip for the development of Optical and 3D Network-On-Chip Architectures.

DETAILED SYLLABUS:

Unit – I: Introduction to NoC (Hours: 10)
Introduction to NoC, OSI layer rules in NoC, Interconnection Networks in Network-on-Chip Network Topologies, Switching Techniques, Routing Strategies, Flow Control Protocol Quality-of-Service Support-Optical NOC.

Unit – II: Architecture Design (Hours: 09)
Switching Techniques and Packet Format, Asynchronous FIFO Design, GALS Style of Communication, Wormhole Router Architecture Design, VC Router Architecture Design, Adaptive Router Architecture Design.

Unit – III: Routing Algorithm (Hours: 10)

Packet routing-QoS, congestion control and flow control, router design, network link design, Efficient and Deadlock-Free Tree-Based Multicast Routing Methods, Path-Based Multicast Routing for 2D and 3D Mesh Networks, Fault-Tolerant Routing Algorithms, Reliable and Adaptive Routing Algorithms.

Unit – IV: Test and Fault Tolerance Of NOC (Hours: 08)

Design-Security in Networks-on-Chips, Formal Verification of Communications in Networks, on-Chips Test and Fault Tolerance for Networks-on-Chip Infrastructures, Monitoring Services for Networks-on Chips.

Unit – V: Three-Dimensional Integration of Network-On-Chip (Hours: 08)

Three-Dimensional Networks-on-Chips Architectures, A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures, Resource Allocation for QoS On-Chip Communication, Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on Chip.

Total Hours: 45

TEXT BOOK:

1. Chrysostomos Nicopoulos, Vijay krishnan Narayanan, Chita R.Das, "*Networks-on – Chip Architectures Holistic Design Exploration*", Springer.1st Edition, 2010.

REFERENCE BOOKS:

1. Fayezge bali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi *"Networks-on-Chips theory and practice",* 1ST Edition,2017CRC press.
2. Konstantinos Tatas and Kostas Siozios "*Designing 2D and 3D Network-on-Chip Architectures"* 1ST Edition,2014.
3. Palesi, Maurizio, Daneshtalab, Masoud "*Routing Algorithms in Networks-on-Chip"* 1ST Edition ,2014.
4. Santanu Kundu, Santanu Chattopadhyay "*Network-on-Chip: The Next Generation of System on-Chip Integration*", 1ST Edition,2017 CRC Press.

ADDITIONAL LEARNING RESOURCES

1. https://www.hindawi.com/journals/jece/2012/509465/
2. https://nptel.ac.in/courses/106103183/22

M. Tech. – II Semester
(19MT25731) PHYSICAL DESIGN AUTOMATION LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:

Graph Algorithms, Partitioning Algorithms, Floorplanning Algorithms, Routing Algorithms.

COURSE OBJECTIVES:

CEO1: To impart knowledge on modeling Design automation algorithms.
CEO2: To develop programming skills to solve problems in designing algorithms for Optimizing Physical Designs.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Demonstrate hands-on experience on modeling design automation algorithms by using the related EDA Tools.
CO2. Design and develop algorithms for optimizing physical designs.
CO3. Work individually and in groups to solve problems with effective communication.

List of Exercises/Experiments: (10-12 Exercises/Experiments)

1. Model the pseudo code for Depth First graph search algorithms for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

2. Model the pseudo code for Breadth First graph search algorithms for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

3. Model the pseudo code for spanning tree algorithm (Kruskal's Algorithm) for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

4. Model the pseudo code for shortest path algorithm (Dijkstra Algorithm) for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

5. Model the pseudo code for Steiner tree algorithm for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

6. Model the pseudo code for Kernighan-Lin Partitioning algorithm for optimization of

designs using EDA Tool and assess the parameters like cut-size, gain, area, etc.

7. Model the pseudo code for Simulated Annealing Partitioning algorithm for optimization of designs using EDA Tool and assess the parameters like cut-size, gain, area, etc.

8. Model the pseudo code for Constraint based Floorplanning algorithm for optimization of designs using EDA Tool and assess the parameters like area, contingency, etc.

9. Model the pseudo code for Integer Programming based Floorplanning algorithm for optimization of designs using EDA Tool and assess the parameters like area, contingency, etc.

10. Model the pseudo code for two terminal routing algorithm for optimization of designs using EDA Tool and assess the parameters like area, delay, etc.

11. Model the pseudo code for Lee's Maze routing algorithm for optimization of designs using EDA Tool and assess the parameters like area, delay, etc.

12. Model the pseudo code for Line Probe routing algorithm for optimization of designs using EDA Tool and assess the parameters like area, delay, etc.

13. Mini Projects (MPs):
    Form a group of maximum 2 members as a team and assign mini projects related to Development of algorithms for compaction of layouts.

REFERENCE BOOKS/LABORATORY MANUALS

1. ECE Department Physical Design Automation Lab Manual.
2. Naveed Shervani, "*Algorithms for Physical Design Automation*", 3rd Edition, Kluwer Academic, 1998.
3. Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, *"Handbook of Algorithms for Physical Design Automation"*, CRC Press,2008.

SOFTWARE/Tools used:

Cadence/synopsys/mentor graphics

ADDITIONAL LEARNING RESOURCES

1. https://nptel.ac.in/noc/individual_course.php?id=noc17-cs15

M. Tech. – II Semester
(19MT2AC01) STATISTICS WITH R
(Audit Course)
(Common to All M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	2	-	-	-

PRE-REQUISITES: A course on Statistics.

COURSE DESCRIPTION:
Concepts of R programming basics, Bivariate and multivariate data, Confidence intervals, Goodness of fit, Analysis of variance.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Import, manage, manipulate, and structure data files using R programming.
CO2. Implement models for statistical analysis of a given dataset and visualize the results to identify trends, patterns and outliers in data.

DETAILED SYLLABUS:

UNIT I - INTRODUCTION (Hours : 05)
Data, R's command line, Variables, Functions, The workspace, External packages, Data sets, Data vectors, Functions, Numeric summaries, Categorical data.

Unit II - BIVARIATE AND MULTIVARIATE DATA (Hours : 07)
Lists, Data frames, Paired data, Correlation, Trends, Transformations, Bivariate categorical data, Measures of association, Two-way tables, Marginal distributions, Conditional distributions, Graphical summaries, Multivariate data - Data frames, Applying a function over a collection, Using external data, Lattice graphics, Grouping, Statistical transformations.

UNIT III - POPULATIONS (Hours : 06)
Populations, Discrete random variables, Random values generation, Sampling, Families of distributions, Central limit theorem, Statistical Inference - Significance tests, Estimation, Confidence intervals, Bayesian analysis.

UNIT IV - CONFIDENCE INTERVALS (Hours : 06)
Confidence intervals for a population proportion, p - population mean, Other confidence intervals, Confidence intervals for differences, Confidence intervals for the median, Significance test - Significance test for a population proportion, Significance test for the mean (t-tests), Significance tests and confidence intervals, Significance tests for the median.

UNIT V - GOODNESS OF FIT (Hours : 06)

The chi-squared goodness-of-fit test, The multinomial distribution, Pearson's χ^2-statistic, chi-squared test of independence and homogeneity, Goodness-of-fit tests for continuous distributions, ANOVA - One-way ANOVA, Using *lm* for ANOVA.

Total Hours: 30

TEXT BOOKS:

1. John Verzani, *Using R for Introductory Statistics*, CRC Press, 2nd Edition, 2014.
2. Sudha G Purohit, Sharad D Gore, Shailaja R Deshmukh, *Statistics Using R*, Narosa Publishing house, 2nd Edition, 2015.

REFERENCE BOOKS:

1. Francisco Juretig, *R Statistics Cookbook*, Packt Publishing, 1st Edition, 2019.
2. Prabhanjan N. Tattar, Suresh Ramaiah, B. G. Manjunath, *A Course in Statistics with R*, Wiley, 2018.