SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)

Sree Sainath Nagar, Tirupati

Department of Electronics and Communication Engineering

Supporting Document for 1.1.2

Syllabus Revision carried out in 2016

Program: M.Tech.-VLSI

Regulations : SVEC-16

This document details the following:

1. Courses where syllabus has been changed 20% and more.
2. Course-wise revised syllabus with changes highlighted.

Note: *For SVEC-16 revised syllabus, SVEC-14 (previous syllabus) is the reference.*

List of Courses where syllabus content has been changed (20% and more)

S. No.	Course Code	Name of the course	Percentage of content changed	Page Number in which Details are Highlighted
1.	16MT15701	Analog IC Design	20	3
2.	16MT15704	Digital IC Design	40	7
3.	16MT23808	Real Time Systems	100	11
4.	16MT15706	Advanced Digital Signal Processing	20	13
5.	16MT15707	FPGA Architectures and Applications	60	17
6.	16MT15708	RFIC Design	100	21
7.	16MT15731	Analog IC Design Lab	70	23
8.	16MT15732	Digital IC Design Lab	20	27
9.	16MT13808	Research Methodology	100	31
10.	16MT25703	Nanoelectronics	100	33
11.	16MT13806	ASIC Design	60	35
12.	16MT25708	System-on-Chip Design and Verification	100	39
13.	16MT25731	Mixed Signal and Physical Design Automation Lab	30	41
14.	16MT25732	Nanoelectronics Lab	100	45
15.	16MT23810	Intellectual Property Rights	100	46
		Average %**(A)**	80.77	-
		Total No. of Courses in the Program **(T)**	28	
		No. of Courses where syllabus (more than 20% content) has been changed **(N)**	15	
		Percentage of syllabus content change in the courses **(C)=(A x N)/100**	12.12	
		Percentage of Syllabus Content changed in the Program (P)= C/T	**43.29**	

DEAN (Academics)

DEAN (Academic)
SREE VIDYANIKETHAN ENGINEERING COLLEGE
Sree Sainath Nagar, A. RANGAMPET
CHITTOOR (DT.)-517 102, A.P.

PRINCIPAL

PRINCIPAL
SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. RANGAMPET
Chittoor (Dist.) - 517 102, A.P., INDIA.

M. Tech. - I SEMESTER
(16MT15701) ANALOG IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:

Courses on Semiconductor Devices and Circuits and VLSI design at UG Level.

COURSE DESCRIPTION:

MOS Device physics; Characteristics of amplifiers; Feedback circuits and operational amplifiers; Stability and frequency compensation of operational amplifiers; Nonlinear Analog circuits & other applications

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
   - Sub threshold and Short Channel effects.
   - Current Mirrors.
   - Frequency response and Noise Characteristics of Amplifier.
   - Effect of Loading in Feedback Circuits.
   - One stage operational Amplifiers.
   - Ring Oscillator.
2. Analyze complex engineering problems critically in the domain of analog IC design for conducting research.
3. Design analog integrated Circuits for societal needs.
4. Develop Skills to solve engineering problems for feasible and optimal solutions in the core area of analog ICs.
5. Initiate research work on Reusable Design for the development of analog IC design.
6. Apply appropriate technique to implement accurate models for devices.

Detailed Syllabus:

Unit-I: Basic MOS Device Physics and Single Stage Amplifiers (Periods: 15)
Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second-Order Effects.
Single Stage Amplifiers: Basic Concepts, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential Amplifiers-Single Ended and Differential Operation, Basic Differential Pair. Passive and Active Current Mirrors.

Unit-II: Frequency Response and Noise Characteristics of Amplifiers
(Periods: 08)
Frequency Response-General Considerations, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential pair.
Noise-Statistical Characteristics of Noise, Noise in Single Stage Amplifiers, Noise in Differential Pairs.

Unit-III: Feedback Circuits and Operational Amplifiers (Periods: 12)
Feedback Circuits - General considerations, Feedback Topologies, Effect of Loading, Effect of Feedback on Noise.

Operational Amplifiers - General considerations, One-stage Op Amps, Two - stage Op Amps, Gain Boosting, Input range limitations, slew rate, power supply rejection, Noise in Op Amps.

Unit-IV: Stability & Frequency Compensation and Bandgap References

(Periods:10)

Stability & Frequency Compensation: General considerations, Multi pole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps.

Bandgap References: Supply-Independent Biasing, Temperature-independent References, PTAT Current Generation, Constant - Gm Biasing, Speed and Noise Issues.

Unit-V: Nonlinear Analog circuits & other applications (Periods: 10)

Sampling Switches, Switched-Capacitor Amplifiers, Switched capacitor integrator, Ring oscillators, Simple PLL.

Total Periods: 55

TEXT BOOK:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata McGraw-Hill, 14th Reprint 2008.

REFERENCE BOOKS:

1. D.A. John & Ken Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.
2. Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.

M. Tech. (VLSI)-I Semester

(14MT15701) ANALOG IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
Courses on Semiconductor Devices and Circuits and Linear IC Applications at UG Level

COURSE DESCRIPTION:
Device physics; Characteristics of amplifiers; Feedback circuits and operational amplifiers; Stability and frequency compensation of operational amplifiers; Switched capacitor circuits.

COURSE OBJECTIVES:

CEO1. To impart in-depth knowledge in analog VLSI Circuits.

CEO2. To provide analytical, logical, design and development skills in OP-Amps, Transistor current mirrors and switched capacitor circuits.

CEO3. To apply knowledge and skills pertaining to analog ICs to solve the real-world problems.

COURSE OUTCOMES: On completion of course, the student will be able to

CO1. Gain advanced knowledge in
- Current Mirrors
- Effect of Loading in Feedback Circuits
- One stage operational Amplifiers
- Switched-Capacitor Circuits

CO2. Analyze complex engineering problems critically in the domain of analog IC design for conducting research.

CO3. Solve engineering problems for feasible and optimal solutions in the core area of analog ICs.

CO4. Apply appropriate techniques to engineering problems in the filed of analog IC design.

DETAILED SYLLABUS

UNIT- I: (Periods: 14)

Basic MOS Device Physics:
General Considerations, MOS I/V Characteristics, Second-Order Effects, MOS Device Models.

Single Stage Amplifiers:
Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential Amplifiers and Current Mirrors.

UNIT- II: FREQUENCY RESPONSE AND NOISE CHARACTERISTICS OF AMPLIFIERS (Periods:07)

Frequency Response-General Considerations, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential pair. Noise- Statistical Characteristics of Noise, Noise in Single Stage Amplifiers, Noise in Differential Pairs.

UNIT- III: FEEDBACK CIRCUITS AND OPERATIONAL AMPLIFIERS (Periods: 12)

Feedback Circuits- General considerations, Feedback Topologies, effect of loading, Effect of Feedback on Noise.

Operational Amplifiers- General considerations, One-stage Op Amps, Two - stage Op Amps, Gain boosting, Input range limitations, slew rate, power supply rejection, Noise in Op Amps.

UNIT- IV: (Periods: 08)

Stability and Frequency Compensation:

General considerations, Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps, Other Compensation Techniques.

Bandgap References:

Supply-Independent Biasing, Temperature-independent References, PTAT Current Generation, Constant - Gm Biasing, Speed and Noise Issues.

UNIT- V: INTRODUCTION TO SWITCHED–CAPACITOR CIRCUITS (Periods: 09)

General Considerations, Sampling Switches, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitors Common-Mode Feedback.

Total periods: 51

TEXT BOOKS:

1: Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata-McGraw-Hill, 2002.

REFERENCE BOOKS:

1: D.A.John & Ken Martin, "Analog Integrated Circuit Design", John Wiley, 1997.

2: Philip Allen & Douglas Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.

M. Tech. I - Semester
(16MT15704) DIGITAL IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on Digital IC Applications and VLSI Design at UG Level.

COURSE DESCRIPTION:
Introduction to MOS transistors; Characteristics of CMOS digital circuits; Transistor sizing; memory design; Design strategies; Design of subsystems.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Gain in-depth knowledge in
   - Static and dynamic characteristics of CMOS.
   - Alternative CMOS Logics
   - Transistor sizing
   - Adders Design
   - Design rules to develop layouts
   - Estimation of Delay and Power
2. Analyze complex engineering problems critically in the domain of CMOS Digital Integrated Circuits for conducting research.
3. Solve engineering problems for feasible and optimal solutions in the core area of CMOS Digital ICs.
4. Initiate research in Digital IC Applications.
5. Apply the Digital CMOS techniques for usage of modern CAD tools and their Limitations.
6. Contribute to multidisciplinary scientific work in the field of modern digital circuits like processor, memory designs.

DETAILED SYLLABUS:

UNIT I – CMOS INVERTER CHARACTERSTICS AND DESIGN STYLES (11 periods)

MOS INVERTERS: Introduction, Definitions and Properties, Static CMOS Inverter, Static and Dynamic Power Dissipation, CMOS inverter delay time definitions and calculations
DESIGNINGCOMBINATIONAL LOGIC GATES in CMOS: Introduction, Static CMOS Design, Dynamic CMOS Design, Domino and NORA logic, Power Consumption in CMOS Gates.

UNIT II – DESIGNING SEQUENTIAL LOGIC GATES in CMOS (12 periods)
Introduction, Static Sequential Circuits, Dynamic Sequential Circuits, Non-Bistable Sequential Circuit, Logic Style for Pipelined Structures.
Timing Issues in Digital Circuits: Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization.

UNIT III – HIGH SPEED NETWORK AND MEMORY DESIGN (11 periods)
Methods of Logical Effort for transistor sizing -Power consumption in CMOS Gates, Low power CMOS design. CMOS Memory design – SRAM, DRAM.

UNIT IV – SUBSYSTEM DESIGN PROCESS (11 periods)

General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Multipliers, modified Booth's algorithm.

UNIT V – DESIGN METHODOLOGY AND TOOLS (10 periods)

Introduction, Structured Design Strategies, Design Methods, Design Flows, Design Economics, Data Sheets and Documentation.

Total Periods: 55

TEXT BOOKS:

1. Jan M Rabaey, "Digital Integrated Circuits", Pearson Education, 2nd Edition, 2003.
2. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits" McGraw Hill, 3rd edition, 2003.
3. Kamran Eshranghian, Douglas A. Puknell and Sholeh Eshranghian "Essential of VLSI Circuits and Systems", PHI, 1st edition, 2005.
4. Neil H. E. Weste, David Money Harris, "CMOS VLSI Design-A Circuit and Systems Perspective", Pearson Education, 4th Edition, 2011.

REFERENCE BOOKS:

1. Eugene D. Fabricus, "Introduction to VLSI Design", McGraw-Hill International Edition, 1990.
2. John P. Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley & Sons, 2002.

M. Tech. (VLSI)-I Semester

(14MT15704) DIGITAL IC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Digital IC Applications and VLSI Design at UG Level.

COURSE DESCRIPTION:
Design styles and characteristics of CMOS digital circuits; Transistor sizing and memory design; Design strategies; Layout design rules; Design of sub-systems.

COURSE OBJECTIVES:
CEO1: To impart advanced Knowledge in design of CMOS digital Integrated Circuits.
CEO2: To analyze, design, develop and implement layouts of various CMOS Circuits.
CEO3: To apply knowledge and skills pertaining to digital IC design to solve the real-world problems.

COURSE OUTCOMES: On successful completion of this course the students will be able to
CO1 : Gain advanced knowledge in
- Static and dynamic characteristics of CMOS.
- Alternative CMOS Logics
- Transistor sizing
- Adders Design
- Design rules to develop layouts
- Estimation of Delay and Power

CO2: Analyze complex engineering problems critically in the domain of CMOS Digital Integrated Circuits for conducting research.
CO3: Solve engineering problems for feasible and optimal solutions in the core area of CMOS Digital ICs.
CO4: Apply the CMOS Digital IC concepts for usage of modern CAD tools and their Limitations.

DETAILED SYLLABUS:
UNIT I: CMOS INVERTERS CHARACTERSTICS AND DESIGN STYLES (9 Periods)
Static and Dynamic characteristics, Static and Dynamic CMOS design- Domino and NORA logic - Combinational and Sequential circuits.
UNIT II: **HIGH SPEED NETWORK AND MEMORY DESIGN** (9 Periods)
Methods of Logical Effort for transistor sizing -Power consumption in CMOS Gates, Low power CMOS design. CMOS Memory design – SRAM, DRAM.

UNIT III: **DESIGN METHODOLOGY AND TOOLS** (10 Periods)
Introduction, Structured Design Strategies, Design Methods, Design Flows, Design Economics, Data Sheets and Documentation.

UNIT IV: **LAYOUT DESIGN RULES** (11 Periods)

Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT V: **SUBSYSTEM DESIGN PROCESS** (11 Periods)

General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Multipliers, modified Booth's algorithm.

TEXT BOOKS:

1: Eugene D Fabricus, "Introduction to VLSI Design, "McGraw Hill International Edition, 1990

2: Kamran Eshranghian, Douglas A.Puknell and Sholh Eshranghian"Essential of VLSI Circuits and Systems", PHI, 1st edition, 2005.

3: Neil H. E. Weste, David Money Harris, "CMOS VLSI Design-A Circuit and Systems Perspective", Pearson 4th Edition, 2011.

REFERENCE BOOKS:

1: John P.Uyemura, "Introduction to VLSI Circuits and Systems", Wiley Edition, 2002.

2: Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", McGraw Hill, 2nd edition, 1999.

3: Jan M Rabaey, "Digital Integrated Circuits-A Design Perspective", Prentice Hall, 1st edition, 1997.

M.Tech. – I Semester
(16MT23808) REAL TIME SYSTEMS
(PE-I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
Courses on Digital system design, Operating systems and embedded systems.

COURSE DESCRIPTION:
Real time system reference model; Real time scheduling approaches; Fault tolerant real time systems; Real time operating system concepts; Commercial RTOS.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Demonstrate advanced knowledge in
   - Characterizing Real Time Systems
   - Various Scheduling approaches
   - Fault tolerant techniques
   - Real Time Operating System Services
2. Analyze critically various Operating Systems using Contemporary bench marks.
3. Consider trade-offs in Real Time System designing to solve engineering problems to exhibit specific behavior, given a set of performance goals and technology.
4. Familiarize with fault tolerant and scheduling techniques to overcome ever increasing embedded system design complexity combined with reduced time-to-market window to revolutionize embedded system design process.
5. Initiate research in Real Time Systems.
6. Explore tools and derive pseudo code using RTOS, for developing efficient embedded Systems.
7. Carry out multidisciplinary research in designing RTOS based systems.

DETAILED SYLLABUS:

UNIT-I: REAL TIME SYSTEMS (Periods: 10)
Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems- Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency. Functional Parameters, Resource Parameters of Jobs and Parameters of Resources, Scheduling hierarchy.

UNIT-II: APPROACHES TO REAL TIME SCHEDULING (Periods: 10)
Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs Static Systems, Effective Release Times and Dead Lines, Optimality and Non-optimality of EDF and LST algorithms, Challenges in Validating Timing Constraints in Priority Driven Systems, Offline Vs Online Scheduling.

UNIT-III: (Periods: 12)
Scheduling Real Time Tasks in Multiprocessor and Distributed Systems: Multiprocessor task allocation, Dynamic allocation of tasks, Fault tolerant scheduling of tasks, Clocks in distributed Real Time Systems.
Fault Tolerance Techniques: Introduction, Failures- Causes, Types, Detection. Fault and Error Containment, Redundancy- Hardware, Software, Time. Integrated Failure Handling.

UNIT-IV: OPERATING SYSTEMS (Periods: 12)

Overview- Threads and Tasks, the Kernel. Time Services and Scheduling Mechanisms, Basic Operating System Functions- Communication and Synchronization, Event Notification and Software Interrupt Memory Management, I/O and Networking. Processor Reserves and Resource Kernel, Capabilities of Commercial Real Time Operating Systems.

UNIT-V: COMMERCIAL REAL TIME OPERATING SYSTEMS (Periods: 12)

UNIX as RTOS - non preemptive kernel, Dynamic Priority levels and deficiencies. UNIX based Real Time Operating Systems - Extension to UNIX kernel, Host Target Approach, Preemption Point Approach, Self host systems. Windows as RTOS- features of Windows NT, Shortcomings, Windows NT vs UNIX. POSIX - Open software, Genesis of POSIX, Overview of POSIX, Real Time POSIX standard. Survey of Contemporary Real Time Operating Systems- PSOS, VRTX, VXworks, QNX, µC/OS-II, RT Linux, Lynx, Windows CE. Bench-marking Real Time Systems.

Total Periods: 56

TEXT BOOKS:

1. Jane W.S. Liu, "Real Time Systems", Pearson Education, 1st edition, April 2000.
2. C. M. Krishna, Kang G Shin, "Real Time Systems", McGraw-Hill Higher education, 1997.
3. Rajib Mall, "Real Time Systems-Theory and Practice", Pearson Education India, 1st edition, Nov.2012.

REFERENCE BOOKS:

1. Phillip A. Laplante and Seppo J. Ovaska, "Real-Time Systems Design and Analysis: Tools for the Practitioner", Wiley-IEEE Press, 4th edition, Nov. 2011.
2. Hermann Kopetz, "Real-Time Systems: Design Principles for Distributed Embedded Applications ", Springer; 2nd edition, 2011.

I M. Tech. – I Semester
(16MT15706) ADVANCED DIGITAL SIGNAL PROCESSING
(Common to VLSI (PE – I) & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES: Courses on Digital Signal Processing at UG level

COURSE DESCRIPTION:
Digital filter banks; Parametric and Non-Parametric Power Spectrum Estimation methods; computationally efficient algorithms; Applications of DSP.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Gain in-depth knowledge in
   - Filter banks and Wavelets
   - Linear Prediction
   - Efficient power Spectral Estimation Techniques
   - Applications of Multirate signal processing
2. Analyze complex engineering problems critically in the field of Signal Processing.
3. Design optimum filters, multirate DSP systems and computationally efficient DSP algorithms for societal needs.
4. Solve engineering problems for feasible and optimal solutions in the field of digital signal processing.
5. Initiate research in advanced digital signal processing.
6. Learn and apply appropriate techniques, including prediction and modeling to complex engineering activities with an understanding of the limitations.
7. Contribute to scientific research in Radar signal processing ,Inter disciplinary areas like Speech and Image processing and Remote sensing with objectivity and rational analysis.

DETAILED SYLLABUS:

UNIT-I: MULTIRATE FILTER BANKS (Periods:12)
Decimation, Interpolation, Sampling rate conversion by a rational factor I/D, Multistage Implementation of sampling rate conversion. **Digital Filter Banks**: Two-Channel Quadrature-Mirror Filter Bank, Elimination of aliasing, condition for Perfect Reconstruction, Polyphase form of QMF bank, Linear phase FIR QMF bank, IIR QMF bank, Perfect Reconstruction Two-Channel FIR QMF Bank.

UNIT-II: POWER SPECTRAL ESTIMATIONS (Periods:12)
Estimation of spectra from finite duration observation of signals.

Non-Parametric Methods: Bartlett, Welch, Blackman & Tukey methods. Performance Characteristics of Non-parametric Power Spectrum Estimators, Computational Requirements of Non-parametric Power Spectrum Estimates.

Parametric Methods of Power Spectral Estimation:
Auto correlation & Its Properties, Relationship between auto correlation & model parameters, Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT-III: LINEAR PREDICTION (Periods:10)

Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters.

UNIT-IV: DSP ALGORITHMS (Periods:10)

Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT-V: APPLICATIONS OF DIGITAL SIGNAL PROCESSING (Periods:11)

Digital cellular mobile telephony, Adaptive telephone echo cancellation, High quality A/D conversion for digital Audio, Efficient D/A conversion in compact hi-fi systems, Acquisition of high quality data, Multirate narrow band digital filtering, High resolution narrow band spectral analysis.

Total periods: 55

TEXT BOOKS:

1. John G. Proakis, Dimitris G. Manolakis, *Digital signal processing, principles, Algorithms and applications,* Prentice Hall, 4th edition, 2007.
2. Sanjit K Mitra, "*Digital signal processing, A computer base approach",* McGraw-Hill Higher Education, 4th edition, 2011.

REFERENCE BOOKS:

1. Emmanuel C Ifeacher Barrie. W. Jervis, "*DSP-A Practical Approach*", Pearson Education, 2nd edition, 2002.
2. A.V. Oppenheim and R.W. Schaffer, "*Discrete Time Signal Processing",* PHI, 2nd edition, 2006.

M. Tech. (VLSI) - I Semester (Elective-I)
M. Tech. (CMS) - I Semester

(14MT15706) ADVANCED DIGITAL SIGNAL PROCESSING

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES: Courses on Digital Signal Processing at UG level.

COURSE DESCRIPTION:
Design of digital filter banks; Power spectral estimation; Digital signal processing algorithms; DSP applications.

COURSE OBJECTIVES:

CEO1. To impart advanced knowledge in Digital Signal Processing and applications.
CEO2. To develop skills in design, analysis, problem solving and research in designing Multirate filter banks and power spectral estimation methods.
CEO3. To apply knowledge and skills for development of new algorithms in signal processing.

COURSE OUTCOMES:
On successful completion of this course the students will be able to

CO1. Gain advanced knowledge in
- Filter banks and Wavelets
- Efficient power Spectral Estimation Techniques.
- Adaptive filters.
- Applications of Multirate signal processing

CO2. Analyze complex engineering problems critically for conducting research in Adaptive filter design.

CO3. Solve engineering problems by designing computationally efficient DSP algorithms for feasible and optimal solutions in digital signal processing field.

CO4. Contribute to scientific research in signal processing and inter disciplinary areas like cellular mobile communications, multirate signal processing and spectral analysis.

DETAILED SYLLABUS:

UNIT I: MULTIRATE FILTER BANKS **(Periods:12)**

Decimation, Interpolation, Sampling rate conversion by a rational factor I/D, Multistage Implementation of sampling rate conversion. **Digital Filter Banks**: Two-Channel Quadrature-Mirror Filter Bank, Elimination of aliasing, condition for Perfect Reconstruction, Polyphase form of QMF bank, Linear phase FIR QMF bank, IIR QMF bank , Perfect Reconstruction Two-

Channel FIR QMF Bank .

UNIT II: POWER SPECTRAL ESTIMATIONS (Periods:11)

Estimation of spectra from finite duration observation of signals, **Non-Parametric Methods**: Bartlett, Welch, Blackmann & Tukey methods. Performance Characteristics of Nonparametric Power Spectrum Estimators, Computational Requirements of Nonparametric Power Spectrum Estimates.

UNIT III: PARAMETRIC METHODS OF POWER SPECTRAL ESTIMATION (Periods:11)

Autocorrelation & Its Properties, Relation between auto correlation & model parameters, Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT IV: DSP ALGORITHMS (Periods:10)

Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNITV: APPLICATIONS OF DIGITAL SIGNAL PROCESSING (Periods:11)

Digital cellular mobile telephony, Adaptive telephone echo cancellation, High quality A/D conversion for digital Audio, Efficient D/A conversion in compact hi-fi systems, Acquisition of high quality data, Multirate narrow band digital filtering, High resolution narrowband spectral analysis.

Total periods: 55

TEXT BOOKS:

1. John G. Proakis, Dimitris G. Manolakis, *Digital signal processing, principles, Algorithms and applications,* Prentice Hall, 4th Edition, 2007.
2. Sanjit K Mitra, "*Digital signal processing, A computer base approach",* McGraw-Hill Higher Education, 4th Edition, 2011.

REFERENCE BOOKS:

3. Emmanuel C Ifeacher Barrie. W. Jervis, "*DSP-A Practical Approach*", Pearson Education, 2nd Edition, 2002.
4. A.V. Oppenheim and R.W. Schaffer, "*Discrete Time Signal Processing",* PHI, 2nd Edition, 2006.

M. Tech. – I Semester
(16MT15707) FPGA ARCHITECTURES & APPLICATIONS
(PE - I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
Fundamentals of Programmable devices; Logic Implementation using PLDs and FPGAs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - Programmable Logic Devices
   - Different FPGA Architectures
   - Digital Implementation using FPGA
   - FPGA Applications
2. Analyze complex problems critically for digital implementation issues, to conduct research in Digital VLSI Design.
3. Solve engineering problems with wide range of solutions in FPGA Implementation.
4. Initiate research methodologies in Modeling, Simulation and Implementation of complex engineering applications in the field of Digital Design at different levels of abstraction.
5. Apply appropriate techniques, Resources and tools in, Modeling complex engineering applications with an understanding of limitations.
6. Contribute to multidisciplinary scientific work in the field of FPGA Devices.

DETAILED SYLLABUS

UNIT–I: **Programmable logic Devices** **(Periods: 08)**
Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA Features, Architectures and Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT – II: FPGAs **(Periods: 12)**
Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs, Introduction to advanced FPGAs-Xilinx Virtex and ALTERA Stratix

UNIT -III: **(Periods: 14)**
Finite State Machines (FSM): Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.
FSM Architectures: Architectures centered around non registered PLDs, Design of state machines centered around shift registers, One Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.

UNIT – IV: System Level Design: (Periods: 12)

Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs. System level design using mentor graphics/Xilinx EDA tool (FPGA Advantage/Xilinx ISE), Design flow using FPGAs.

UNIT – V: Case studies (Periods: 09)

Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers

Total periods: 55

TEXT BOOKS:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.
2. Richard F. Tinder, "Engineering Digital Design", Academic Press, 2nd edition, 2000.
3. Charles H. Roth, "Fundamentals of logic design", Thomson/Brooks/Cole, 5th edition, 2004.

REFERENCE BOOKS:

1. Pak K. Chan & Samiha Mourad, "Digital Design Using Field Programmable Gate Array", PTR Prentice Hall, 1st edition, 1994.
2. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, "Field Programmable Gate Array", Kluwer Academic Publishers, 1st edition, 1992.

M. Tech. (VLSI)-I Semester (Elective-I)

(14MT15707) FPGA APPLICATIONS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
Course on VLSI Design at UG Level

COURSE DESCRIPTION:
Families of Field Programmable Gate Arrays; Embedded processors using FPGA; Applications of FPGAs - Motor control, FIR and IIR filters.

COURSE OBJECTIVES:

CEO1. To provide in-depth knowledge in architectures and applications of various Families of FPGAs.

CEO2. To analyze, design, implement and verify FPGAs.

CEO3. To apply knowledge in the design of Embedded Processor, Motor Control, FIR and IIR Digital Filters.

COURSE OUTCOMES: On completion of the course, student will be able to

CO1. Acquire in-depth knowledge in
- FPGAs Design & Architecture.
- Motor Control with FPGAs.
- FIR and IIR Digital Filter implementation with FPGAs.
- FPGA Fabric Immersed Processors.

CO2. Analyze complex engineering problems critically in Programmable digital systems.

CO3. Develop skills to solve the problems in placement and routing of FPGAs.

CO4. Apply appropriate techniques to engineering problems in the design of FPGAs.

DETAILED SYLLABUS

UNIT- I: (10 periods)

Introduction to Field Programmable Gate Arrays (FPGA):
Evolution of Programmable Devices, About FPGAs, Applications of FPGAs. Programming Technologies in FPGAs.

Xillinx and Actel FPGAs:
Xilinx FPGAs –XC2000, XC3000 and XC4000.Actel FPGAs – Actel ACT-1 and Actel ACT-2. Altera FPGAs, Plessey FPGA, Advanced Micro Devices (AMD) FPGA. FPGA Design Flow. Technology Mapping for FPGAs-Logic Synthesis and Lookup Table Technology Mapping.

UNIT- II: FPGA-BASED EMBEDDED PROCESSOR (07 Periods)

Hardware–Software Task Partitioning, FPGA Fabric Immersed Processors, Interfacing Memory to the Processor, Interfacing Processor with Peripherals, Design Re-use Using On-chip Bus Interface, Creating a Customized Microcontroller.

UNIT- III: MOTOR CONTROL USING FPGA (09 Periods)

Introduction to Motor Drives, Digital Block Diagram for Robot Axis Control-Position Loop, Speed Loop and Power Module. Case Studies for Motor Control-Stepper Motor Controller, Permanent Magnet DC Motor, Brushless DC Motor and Permanent Magnet Rotor (PMR). Prototyping Using FPGAs.

UNIT- IV: FIR DIGITAL FILTERS USING FPGA (14 Periods)

Digital Filters, FIR Filter-FIR Filter with Transposed Structure, Symmetry in FIR Filters and Linear-phase FIR Filters. Designing FIR Filters-Direct Window Design Method and Equiripple Design Method. Constant Coefficient FIR Design-Direct FIR Design, FIR Filter with Transposed Structure and FIR Filters Using Distributed Arithmetic.

UNIT- V: IIR DIGITAL FILTERS USING FPGA (10 Periods)

Introduction to IIR, IIR Digital Filter, IIR Coefficient Computation, IIR Filter Implementation-Finite wordlength effects and Optimization of the Filter Gain Factor. Fast IIR Filter-Time domain Interleaving and Clustered and Scattered Look-Ahead Pipelining.IIR Decimator Design and Parallel Processing.

Total periods: 50

TEXT BOOKS:

1. S.Brown, R.Francis, J.Rose, Z.Vransic, "Field Programmable Gate Array", Kluwer Publication, 1992.
2. Rahul Dubey, "Introduction to Embedded System Design Using Field Programmable Gate Arrays", Springer, 2009.
3. Uwe Meyer-Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer Series, 3rd Edition, 2007.

REFERENCE BOOKS:

1. S.Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.

M. Tech. – I Semester
(16MT15708) RFIC DESIGN
(PE - I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on Analog IC Design at UG Level/ PG Level.

COURSE DESCRIPTION:
Basic Concepts of RF Circuits; Transceiver Architectures; Low Noise Amplifier; Mixers; Oscillators; Power Amplifiers and Phased Locked Loops.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Demonstrate in-depth knowledge in RFIC
   - Basic Concepts.
   - Transceiver Architectures.
   - Low Noise Amplifiers.
   - Mixers.
   - Voltage Controlled Oscillators.
   - Phase Locked Loop.
   - Power Amplifiers.
2. Analyze the problems in Radio Frequency Integrated Circuits.
3. Solve problems in transceiver architectures.
4. Initiate research work on designing RF systems for the wireless communications.
5. Apply appropriate techniques to overcome problem of non-idealities in the design of RFIC circuits, Implement various techniques to arrive at Efficient Designs of RFIC Circuits and Model techniques for Linearization of devices used in RFICs.

DETAILED SYLLABUS

UNIT – I: BASIC CONCEPTS IN RF DESIGN (Periods: 07)
Introduction to RF Design, Units in RF design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

UNIT – II: TRANSCEIVER ARCHITECTURES (Periods: 14)
General considerations, Receiver Architectures-Basic Heterodyne receivers, Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers, Low-IF receivers. Transmitter Architectures-Direct Conversion transmitters, Modern direct conversion Transmitters, Heterodyne Transmitters, Other Transmitter Architectures.

UNIT -III: LNA AND MIXERS (Periods: 10)
General considerations, Problem of input matching, Low Noise Amplifiers design in various topologies, Gain Switching, Band Switching, Mixers-General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversion mixers.

UNIT – IV: OSCILLATORS (Periods: 10)
Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, LC VCOs with wide tuning range, phase noise, Mathematical model of VCOS, Quadrature Oscillators.

UNIT – V: PLL AND POWER AMPLIFIER (Periods: 14)

PLLS-Phase detector, Type-I PLLs, Type-II PLLs, PFD/CP Non-idealities, Phase noise in PLLs, Loop Bandwidth. Power Amplifiers-General considerations, Classification of power amplifiers, High- Efficiency power amplifiers, Cascode output stages, Large signal impedance matching, Linearization techniques, Polar Modulation, Outphasing.

Total periods: 55

TEXT BOOK:

1. Behzad Razavi, "RF Microelectronics", PTR Prentice-Hall, 2nd edition, 1998.

REFERENCE BOOKS:

1. Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd edition, 1998.
2. R. Jacob Baker, Harry W. Li, D.E. Boyce, "CMOS Circuit Design, Layout and Simulation", Wiley, 1997.

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M. Tech. - I Semester
(16MT15731) ANALOG IC DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	--	--	4	2

PRE-REQUISITES:
A Course on Linear IC Applications at UG Level.

COURSE DESCRIPTION:
Modeling and simulation of analog circuits using SPICE.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate knowledge in design of analog circuits.
2. Exhibit skills in SPICE Coding and verification of analog circuits.
3. Solve problems in Modeling and analysis of MOSFETs and OPAMPs.
4. Develop Skills to solve problems of design and analysis of analog circuits.
5. Initiate research in analog IC design.
6. Able to use CAD Tools to arrive at an optimized solution for analog signal design.
7. Contribute positively to multidisciplinary scientific research in design and development of Analog Integrated Circuits to solve problems arising in Integrated circuit Technology.
8. Communicate effectively in Verbal and written form of designs developed.

LIST OF EXERCISES:

Modeling and simulation of Analog Circuits using SPICE

1. Study of MOS Characteristics and Characterization.
2. Design and Simulation of single ended and differential Amplifiers.
3. Design and Simulation of Single Stage Amplifiers (Common Source, Source Follower, Common Gate Amplifier).
4. Design and Simulation of Single Stage Amplifiers (Cascode Amplifier, Folded Cascode Amplifier).
5. Design and Simulation of a Differential Amplifier (with Resistive Load, Current Source Biasing).
6. Design and Simulation of Basic Current Mirror, Cascode Current Mirror and Active Current mirrors.
7. Analysis of Frequency response of various amplifiers (Common Source, Source Follower, Cascode, Differential Amplifier.
8. Design/Simulation/Layout of Telescopic Operational Amplifier/ Folded Cascode Operational Amplifier.
9. Design and Simulation of Switched Capacitor.
10. Design and Simulation of various types of first and second order active filters and its applications.
11. Design and Simulation of full wave precision rectifier using opamp.
12. Design and simulation of basic applications based on opamp.

Total Time Slots: 12

REQUIRED SOFTWARE TOOL:
1. Cadence/Synopsys/Mentor graphics Tools.

REFERENCE BOOKS:

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2001.
2. Ken Martin, Analog Integrated Circuit Design, Wiley Publications, 2002.
3. Analog IC Design Lab manual.

M. Tech. (VLSI)-I Semester
(14MT15721) ANALOG AND DIGITAL IC DESIGN LABORATORY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
25	50	75			4	2

PRE-REQUISITES:

A Course on Digital IC Design and Applications at UG Level.

COURSE DESCRIPTION:

Simulation, synthesis and implementation of digital circuits using HDLs; Modeling and simulation of analog circuits using SPICE.

COURSE OBJECTIVES:

CEO1: To Design Digital Circuits using hardware description languages, perform simulation, synthesis and identify the I/O timing constraints and the required design modifications.

CEO2: To apply knowledge and skills to implement principles in the field of Digital Systems.

COURSE OUTCOMES: On successful completion of the course the students will be able to

CO1: Gain skills in
- SPICE Coding and verification of analog circuits.
- Behavioral system modeling: concurrency and event-driven simulation.
- Digital design modeling using various styles (behavioral, structural and dataflow)
- Designing Combinational and sequential circuits
- Verifying the Functionality of Designed circuits using function Simulator
- Checking for critical path time calculation
- Placement and routing in FPGA
- Implement digital designs on FPGA device for conducting research in the field of Digital Circuits.

CO2: Conceptualize and solve problems in logic verification and timing calculation of Digital circuits.

CO3: Acquire research skills in the domain of Digital Systems.

CO4: Create, develop and use modern CAD tools to analyze problems of RTL, Technology schematic, and system implementation.

CO5: Contribute positively to multidisciplinary scientific research in design and development of Integrated Circuits suited for wide range of applications.

CO6: Perform experiments efficiently in Digital system design to achieve optimization for high device utilization and performance in industrial needs.

DETAILED SYLLABUS:

Modeling and simulation of Analog Circuits using SPICE

1. **Part – I:** **(4 slots)**
   Design and verification of Current Mirror Circuits, Differential Amplifiers, Internal Circuit of OP-AMP, Switched Capacitor Integrator.

Modeling and Functional Simulation of the following digital circuits (with XilinX tools) using VHDL/Verilog Hardware Description Languages

2. **Part-II:** **(4 slots)**
Combinational Logic - Logic Gates, Adders, Encoders, decoders, Multiplexer, Demultiplexer, Comparator, Multipliers, ALU, MAC.

3. Part – III: **(4 slots)**
Sequential Logic – Flip-Flops, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial). Memories and State Machines - Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Instruction Fetch, Instruction Decode.

4. Part-IV: **(2 slots)**
FPGA System Design - Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation on FPGA/CPLD.

Total Slots: 14

REQUIRED SOFTWARE TOOL:

2. Xilinx10.1 ISE and Above for FPGA/CPLDs.

REFERENCE BOOKS:

1. John F. Wakerly, "Digital Design: Principles and Practices", Prentice Hall, Third Edition, 2000.
2. Analog and Digital Design Lab manual.

M. Tech. - I Semester
(16MT15732) DIGITAL IC DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	--	--	4	2

PRE-REQUISITES:
A Course on Digital IC Applications at UG Level.

COURSE DESCRIPTION:
Modeling, Simulation, Synthesis and Implementation of digital circuits using HDLs;

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Demonstrate advanced knowledge in design of digital circuits.
2. Exhibit analytical skills in
   - Behavioral system modeling: concurrency and event-driven simulation.
   - Digital design modeling using various styles (behavioral, structural and dataflow)
   - Designing Combinational and sequential circuits
   - Verifying the Functionality of Designed circuits using function Simulator
   - Checking for critical path time calculation
   - Placement and routing in FPGA
   - Implement digital designs on FPGA device for conducting research in the field of Digital Circuits.
3. Conceptualize and Solve problems in logic verification and timing calculation of Digital circuits.
4. Initiate research in digital IC design.
5. Acquire research skills in the domain of Digital Systems.
6. Create, develop and use modern CAD tools to analyze problems of RTL, Technology schematic, and system implementation.
7. Contribute positively to multidisciplinary scientific research in design and development of Digital Integrated Circuits to solve problems arising in Integrated circuit Technology.
8. Communicate effectively in Verbal and written forms for the designs developed.

LIST OF EXERCISES:

Modeling and Functional Simulation of the following digital circuits (with XilinX tools) using Verilog Hardware Description Languages

Part–I: Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Substractor, Multipliers, Decoders, Address decoders, parity generator, ALU

Part–II: Sequential Logic: D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial), Cyclic Encoder / Decoder.

Part–III: Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs

Part-IV: FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of Mini-Project on FPGA/CPLD

Total Time Slots: 12

REQUIRED SOFTWARE TOOL:

1. Xilinx10.1 ISE and Above for FPGA.

REFERENCE BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan, & Borivoje Nikolic, "Digital Integrated Circuits – A design perspective", Prentice Hall, 3rd Edition, 2008.
2. Digital IC Design Lab manual.

M. Tech. (VLSI)-I Semester
(14MT15721) ANALOG AND DIGITAL IC DESIGN LABORATORY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
25	50	75			4	2

PRE-REQUISITES:

A Course on Digital IC Design and Applications at UG Level.

COURSE DESCRIPTION:

Simulation, synthesis and implementation of digital circuits using HDLs; Modeling and simulation of analog circuits using SPICE.

COURSE OBJECTIVES:

CEO1: To Design Digital Circuits using hardware description languages, perform simulation, synthesis and identify the I/O timing constraints and the required design modifications.

CEO2: To apply knowledge and skills to implement principles in the field of Digital Systems.

COURSE OUTCOMES: On successful completion of the course the students will be able to

CO1: Gain skills in
- SPICE Coding and verification of analog circuits.
- Behavioral system modeling: concurrency and event-driven simulation.
- Digital design modeling using various styles (behavioral, structural and dataflow)
- Designing Combinational and sequential circuits
- Verifying the Functionality of Designed circuits using function Simulator
- Checking for critical path time calculation
- Placement and routing in FPGA
- Implement digital designs on FPGA device for conducting research in the field of Digital Circuits.

CO2: Conceptualize and solve problems in logic verification and timing calculation of Digital circuits.

CO3: Acquire research skills in the domain of Digital Systems.

CO4: Create, develop and use modern CAD tools to analyze problems of RTL, Technology schematic, and system implementation.

CO5: Contribute positively to multidisciplinary scientific research in design and development of Integrated Circuits suited for wide range of applications.

CO6: Perform experiments efficiently in Digital system design to achieve optimization for high device utilization and performance in industrial needs.

DETAILED SYLLABUS:

Modeling and simulation of Analog Circuits using SPICE

5. **Part – I:** **(4 slots)**
   Design and verification of Current Mirror Circuits, Differential Amplifiers, Internal Circuit of OP-AMP, Switched Capacitor Integrator.

Modeling and Functional Simulation of the following digital circuits (with XilinX tools) using VHDL/Verilog Hardware Description Languages

6. **Part-II:** **(4 slots)**

Combinational Logic - Logic Gates, Adders, Encoders, decoders, Multiplexer, Demultiplexer, Comparator, Multipliers, ALU, MAC.

7. Part – III: **(4 slots)**

Sequential Logic – Flip-Flops, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-parallel, parallel-to-serial). Memories and State Machines - Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Instruction Fetch, Instruction Decode.

8. Part-IV: **(2 slots)**

FPGA System Design - Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation on FPGA/CPLD.

Total Slots: 14

REQUIRED SOFTWARE TOOL:

3. Xilinx10.1 ISE and Above for FPGA/CPLDs.

REFERENCE BOOKS:

3. John F. Wakerly, "Digital Design: Principles and Practices", Prentice Hall, Third Edition, 2000.
4. Analog and Digital Design Lab manual.

M. Tech. – I Semester
(16MT13808) RESEARCH METHODOLOGY
(Common to all M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	-	2	-	-

PREREQUISITES: --

COURSE DESCRIPTION:

Overview of Research, research problem and design, various research designs, data collection methods, statistical methods for research, importance of research reports and its types.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Acquire in-depth knowledge on
   - Research design and conducting research
   - Various data collection methods
   - Statistical methods in research
   - Report writing techniques.
2. Analyze various research design issues for conducting research in core or allied areas.
3. Formulate solutions for engineering problems by conducting research effectively in the core or allied areas.
4. Carryout literature survey and apply research methodologies for the development of scientific/technological knowledge in one or more domains of engineering.
5. Select and Apply appropriate techniques and tools to complex engineering activities in their respective fields.
6. Write effective research reports.
7. Develop attitude for lifelong learning to do research.
8. Develop professional code of conduct and ethics of research.

DETAILED SYLLABUS:

Unit-I: Introduction to Research Methodology (Periods: 5)
Objectives and Motivation of Research, Types of Research, Research Approaches, Research Process, Criteria of good Research, Defining and Formulating the Research Problem, Problem Selection, Necessity of Defining the Problem, Techniques involved in Defining a Problem.

Unit-II: Research Problem Design and Data Collection Methods (Periods: 7)
Features of Good Design, Research Design Concepts, Different Research Designs, Different Methods of Data Collection, Data preparation: Processing Operations, Types of Analysis.

Unit-III: Statistics in Research (Periods:6)
Review of Statistical Techniques - Mean, Median, Mode, Geometric and Harmonic Mean, Standard Deviation, Measure of Asymmetry, ANOVA, Regression analysis.

Unit-IV: Hypothesis Testing (Periods: 7)

Normal Distribution, Properties of Normal Distribution, Basic Concepts of Testing of Hypothesis, Hypothesis Testing Procedure, Hypothesis Testing: t-Distribution, Chi-Square Test as a Test of Goodness of Fit.

Unit-V: Interpretation and Report Writing (Periods: 3)

Interpretation – Techniques and Precautions, Report Writing – Significance, Stages, Layout, Types of reports, Precautions in Writing Reports.

Total Periods: 28

TEXT BOOK:

1. C.R. Kothari, "*Research Methodology: Methods and Techniques*," New Age International Publishers, New Delhi, 2nd Revised Edition, 2004.

REFERENCE BOOKS:

1. Ranjit Kumar, "*Research Methodology: A step-by-step guide for beginners*," Sage South Asia, 3rd ed., 2011.
2. R. Panneerselvam, "Research Methodology," PHI learning Pvt. Ltd., 2009

M.Tech. - II Semester
(16MT25703) NANOELECTRONICS

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
Courses on Basic Engineering Physics, Basic Engineering Chemistry and Electronic Devices at UG level.

COUSRE DESCRIPTION:
Introduction to wave particle nature and mechanics; Crystal structure of semiconducting material; Material for nanoelectronics; Different techniques of nanostructure fabrication; Nanostructure Characterization; Electron transport mechanism.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - wave particle nature, wave mechanics,
   - crystal structure of semiconducting material
   - different techniques of nanostructure fabrication,
   - characterization of the nanostructure and electron in well
2. Analyze
   - Crystal structure of nanomaterials
   - Nanostructure based device
3. Design and develop new nanodevices for advanced technological applications.
4. Efficiently solve complex problems in the field of nanoelectronics.
5. Involve and resolve the future research challenges in the fields related to Nanoelectronics.
6. Contribute to multidisciplinary research in biotechnology, MEMS, other nanotechnology fields.

DETAILED SYLLABUS:

UNIT I -PARTICLES AND WAVE MECHANICS (periods: 10)
Introduction classical particles, classical waves, wave–particle duality, Wave mechanics, Schrodinger wave equation, wave mechanics of particles, atoms and atomic orbital's.

UNIT II - MATRIAL FOR NANOELECTRONICS (periods: 10)
Introduction, Semiconductors, Crystal structure and Crystal lattices: bonding in crystals, Electron energy bands, Semiconductor heterostructures, Lattice-matched and pseudomorphic heterostructure, Organic semiconductors, Carbon nanomaterials: nanotubes and fullerenes.

UNIT III - FABRICATION AND CHARACTERISATION OF NANOSTRUCTURES (periods: 12)
Bulk crystal and heterostructure growth, Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices, Characterization techniques of nanostructures, Spontaneous formation and ordering of nanostructures, Nanocrystals and nanoclusters, Methods of nanotube growth, Chemical and biological methods for nanoscale fabrication, Fabrication of nanoelectromechanical systems.

UNIT IV - ELECTRON TRANSPORT AND TRADITIONAL LOW-DIMENSIONAL STRUCTURES (periods: 10)

Electron Transport In Nanostructures

Introduction, Time and length scales of the electrons in solids, Statistics of the electrons in solids and nanostructures, The density of states of electrons in nanostructures, Electron transport in nanostructures.

Electrons In Traditional Low-Dimensional Structures

Introduction, Electrons in quantum wells, Electrons in quantum wires, Electrons in quantum dots.

UNIT V -NANOELECTRONIC DEVICES (periods: 13)

General Properties, Resonant Tunneling Diode, Operating Principle and Technology, Applications in High Frequency and Digital Electronic, Circuits and Comparison with Competitive Devices, Quantum Cascade Laser, Operating Principle and Structure, Quantum Cascade Lasers in Sensing and Ultrafast Free, Space Communication Applications, Single Electron Transistor, Operating Principle, Technology, Applications, Carbon Nanotube Devices Structure and Technology, Carbon Nanotube Transistors.

Total Periods: 55

TEXT BOOKS:

1. V. Mitin, V. Kochelap, M. Stroscio, "Introduction to Nanoelectronics", Cambridge University Press (2008).
2. W.R.Fahrner, "Nanotechnology and Nanoelectronics – Materials, Devices, Measurement Techniques", Springer-Verlag Berlin, Germany (2005).

REFERENCE BOOKS:

1. Supriyo Datta, "Lessons from Nanoelectronics: A New Perspective on Transport", World Scientific Publishing Co. Pte. Ltd. 5 Toh Tuck Link, Singapore 596224, Vol. 1, (2012).
2. Bhushan, Bharat, "Springer Handbook of Nanotechnology", 2nd edition, 2006.

M. Tech. – II Semester
(16MT13806) ASIC DESIGN
(PE-II)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
ASIC design categories; Design Libraries; Design Entry; Logic Synthesis; Simulation; Testing; Physical design flow of ASIC.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Gain in-depth knowledge in
   - ASIC Design Styles.
   - ASICs Design Libraries.
   - ASICs Design Issues.
   - ASIC Construction.
2. Analyze problems critically in the field of ASIC Design.
3. Design Application Specific ICs for use in various systems.
4. Solve engineering problems and arrive at optimal solutions in pertaining to ASIC Design.
5. Initiate research in ASIC Design.
6. Apply appropriate techniques, resources and tools to engineering activities to provide appropriate Solution for the development of ASICs.
7. Contribute to multidisciplinary scientific work in the field of ASIC Design.

DETAILED SYLLABUS:

UNIT-I: INTRODUCTION TO ASICs (Periods: 10)
Types of ASICs- Full-Custom ASICs, Semicustom ASICs, Standard cell based ASICs, Gate-array based ASICs, Channeled Gate Array, Channel less Gate Array, Structured Gate Array, Programmable Logic Devices, Field-Programmable Gate Arrays, ASIC Design Flow, ASIC Cell Libraries.

UNIT-II: ASIC LIBRARY DESIGN & PROGRAMMABLE ASICs (Periods: 10)
ASIC LIBRARY DESIGN: Transistors as Resistors, Transistor Parasitic Capacitance, Logical Effort, Library cell design, Library Architecture, Gate-Array Design, Standard-Cell Design, Data path-Cell Design.
PROGRAMMABLE ASICs: Anti fuse, Static RAM, EPROM and EEPROM technology, Practical Issues, Specifications.

UNIT-III: LOW-LEVEL DESIGN ENTRY & LOGIC SYNTHESIS (Periods: 12)
LOW-LEVEL DESIGN ENTRY: Schematic Entry, Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, Vectored instances and Buses, Edit-in-place, Attributes, Net list Screener, Back-Annotation.
LOGIC SYNTHESIS: A Logic-Synthesis Example**,** Verilog and Logic Synthesis, VHDL and Logic Synthesis, Finite-State Machine Synthesis, Memory Synthesis.

UNIT-IV: SIMULATION, TESTING & ASIC CONSTRUCTION (Periods: 13)

SIMULATION AND TESTING: Types of Simulation -Structural Simulation, Gate-Level Simulation, Static Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation, Boundary Scan Test, Faults, Fault simulation, Automatic Test-Pattern Generation.

ASIC CONSTRUCTION: Physical Design, System Partitioning, FPGA Partitioning, Partitioning Methods.

UNIT-V: FLOOR PLANNING, PLACEMENT & ROUTING (Periods: 10)

FLOOR PLANNING AND PLACEMENT: Floor planning, Placement, Physical Design Flow, **ROUTING:** Global Routing, Detailed Routing, Special Routing, Circuit Extraction and DRC.

Total Periods: 55

TEXT BOOKS:

1. Micheal John Sebastian Smith, "Application - Specific Integrated Circuits", Addison Wesley Professional, 1997.
2. L. J. Herbst, "Integrated circuit engineering", Oxford University Press, 1996.

REFERENCE BOOKS:

1. Neil H.E. Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design: A Systems Perspective", Addison – Wesley Publication Company, 2nd Edition, 1999.
2. John P. Uyemura, "Introduction to VLSI Circuits and Systems", Wiley, 1st Illustrated Edition, 2002.

M. Tech. (VLSI)-II Semester (Elective-II)
(14MT25706) ASIC DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	--	--	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level

COURSE DESCRIPTION:
ASIC design categories; Design issues, characteristics, design techniques, synthesis, testing and physical design flow of ASIC.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in ASIC Design.

CEO2: To provide design, analytical, logical and development skills in high performance ASICs.

CEO3: To apply knowledge and skills pertaining to ASIC design to solve the real-world problems.

COURSE OUTCOMES:

On successful completion of this course the students will be able to
CO1: Gain in-depth knowledge in
- ASIC Design Styles.
- ASICs Design Issues.
- ASICs Design Techniques.
- ASIC Construction.

CO2: Analyze the characteristics and Performance of ASICs and judge independently the best suited device for fabrication of smart devices for conducting research in ASIC design.

CO3: Solve problems of Design issues, simulation and Testing of ASICs.

CO4: Apply appropriate techniques, resources and tools to engineering activities for appropriate Solution to develop ASICs.

DETAILED SYLLABUS:

UNIT-I **(Periods: 11)**
ASIC DESIGN STYLES: Introduction – categories-Gate arrays-Standard cells-Cell based ASICs-Mixed mode and analogue ASICs – PLDs.

ASICS– PROGRAMMABLE LOGIC DEVICES: Overview – PAL –based PLDs: Structures; PAL Characteristics – FPGAs: Introduction, selected families –design outline.

UNIT-II **(Periods: 11)**

ASICS –DESIGN ISSUES: Design methodologies and design tools – design for testability – economies.

ASICS CHARACTERISTICS AND PERFORMANCE: design styles, gate arrays, standard cell -based ASICs, Mixed mode and analogue ASICs.

UNIT-III: ASICS-DESIGN TECHNIQUES **(Periods: 08)**

Overview- Design flow and methodology- Hardware description languages-simulation and checking-commercial design tools- FPGA Design tools: XILINX, ALTERA.

UNIT-IV **(Periods: 13)**

LOGIC SYNTHESIS, SIMULATION AND TESTING: Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test- fault simulation- automatic test pattern generation.

ASIC CONSTRUCTION: Floor planning, placement and routing system partition.

UNIT-V: FPGA PARTITIONING **(Periods: 10)**

Partitioning Methods-Floor Planning- Placement- Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

Total Periods: 53

TEXT BOOKS:

1. L.J.Herbst, “Integrated circuit engineering”, OXFORD SCIENCE Publications, 1996.

REFERENCE BOOKS:

1. M.J.S.Smith, “Application - Specific integrated circuits”, Addison-Wesley Longman Inc 1997.

M. Tech. - II SEMESTER
(16MT25708) SYSTEM-ON-CHIP DESIGN AND VERIFICATION
(PE – II)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:
Courses on Embedded systems and VLSI design.

COURSE DESCRIPTION:
System on Chip Design Process; System level Design Issues; Test Strategies; Macro Design and Verification; Reusable Macros; System on Chip Verification; Communication Architectures for SoCs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
    - System on Chip Design Processes.
    - Macro Level Design.
    - Verification Techniques.
    - On-Chip Communication Architectures.
    - Bus Functional Model based Verification.
2. Analyze the problems in SoC Design for Low Power Architecture Design.
3. Develop Skills to solve problems of Reusable Macros.
4. Initiate research work on Reusable Design for the development of SoC Architectures.
5. Implement various Verification techniques to arrive at Efficient Designs of SoC Architectures.

DETAILED SYLLABUS:

Unit-I: System on Chip Design Process (Periods: 08)
A canonical SoC Design, SoC Design flow- waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification, System Design process, System level design issues - Soft IP Vs Hard IP, Design for timing closure - Logic design issues, Verification strategy, Onchip buses and interfaces, Design for Low Power, Manufacturing test strategies.

Unit-II: Macro Design Process (Periods: 08)
Overview of IP Design, planning and Specification, Macro Design and Verification, Soft Macro Productization, Developing hard macros - Design issues for hard macros, Model Development for Hard Macros. System Integration with reusable Macros.

Unit-III: SoC Verification - I (Periods: 14)
Technology Challenges, Verification technology options, Verification methodology, Testbench Creation, Testbench Migration, Verification languages, Verification IP Reuse, Verification approaches, Verification and Device Test, Verification plans, Bluetooth SoC.
System level verification – System Design, System Verification.
Block level verification – IP Blocks, Block Details of Bluethooth SoC, Lint Checking, Formal Model Checking, Functional Verification/Simulation, Protocol Checking, Directed Random Testing, Code Coverage Analysis.

Unit-IV: SoC Verification - II (Periods: 15)

Hardware/Software Co-verification- HW/SW Co-verification Environment, Emulation, soft or virtual Prototypes, Co-verification, UART Co-verification, Rapid Prototype Systems, Software Testing. Static netlist verification, Physical Verification and Design Signoff, Introduction to VMM (Verification Methodology Manual), OVM(Open Verification Methodology) and UVM (Universal Verification Methodology).

Unit-V: Design of Communication Architectures for SoCs (Periods: 10)

On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures - Communication architecture tuners. Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.

Total Periods: 55

TEXT BOOKS:

1. Michael Keating, Pierre Bricaud, "Reuse Methodology manual for System-On-A-Chip Designs", Kluwer Academic Publishers, 2nd Edition, 2002.
2. Prakash Rashinkar, Peter Paterson, Leena Singh, "SoC Verification Methodology and Techniques", Kluwer Academic Publishers, 2002.
3. Ahmed Amine Jerraya, Wayne Wolf, "Multiprocessor Systems-on-chips", Morgan Kaufmann Publishers, 2005.

REFERENCE BOOKS:

1. William K. Lam, "Hardware Design Verification: Simulation and Formal Method based Approaches", Prentice Hall Professional Technical Reference, 2005.
2. Farzad Nekoogar, Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall Professional, 2003.

M.Tech. – II Semester
(16MT25731) MIXED SIGNAL AND PHYSICAL DESIGN AUTOMATION LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PREREQUISITE:
A course on Circuit Level Design and Layouts.

COURSE DESCRIPTION:
Design and Verification of Analog and Mixed Signal Circuits.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in backend and frontend design.
2. Exhibit analytical skills in
    - Backend Design - Schematic or SPICE Entry, Simulation, Layout, DRC, PEX, Post Layout Simulation.
    - Frontend Design - HDL Design Entry, Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing Simulation, Partition, Floorplanning, Place & Route, Compaction, Verification, Design for Testability, Static Timing Analysis, Power Analysis.
3. Solve problems in physical design cycle, functional verification, timing and Power Analysis of Digital circuits.
4. Initiate research in the field of mixed signal and physical design automation.
5. Develop Skills to solve problems of layout design and build solutions for optimizing design for area, power and speed.
6. Use CAD Tools to arrive at an optimized solution for mixed signal design.
7. Contribute positively to multidisciplinary scientific research in design and development of Mixed/Analog Integrated Circuits to solve problems arising in physical design and Integrated circuit Technology.
8. Communicate effectively in Verbal and written form of designs developed.

LIST OF EXERCISES:
Mentor Graphic tools / Cadence tools / Synopsis tools

1. **Backend Design (4 Slots)**

Schematic Entry, Simulation, Layout, DRC, PEX, Post Layout Simulation of CMOS Logic Gates, Combinational Circuits (Adders, Encoders, Decoders, Multiplexers, Demultiplexers, etc), Sequential Circuits(Flip Flops, Registers, counters),Biquad Filter, PLL, VCO and ADC/DAC.

2. **Frontend/Semicustom Design (4 Slots)**

HDL Design Entry, Logic Simulation, RTL Logic Synthesis, Post Synthesis TimingSimulation, Place & Route, Design for Testability, Static Timing Analysis, PowerAnalysis of Combinational and Sequential Circuits(Application Oriented designs – MAC Unit, FIR and IIR Filters, Traffic Light Controller, FSM based Control applications, etc).

3. **Physical Design Automation (4 Slots)**

Graph Algorithms, Partitioning Algorithms, Floorplanning Algorithms, Routing Algorithms.

Total Time Slots: 12

Required Software Tools:

1. Mentor Graphic tools / Cadence tools / Synopsis tools/MAGMA/MAGIC. (220 nm Technology and Above)
2. Xilinx ISE 10.1i and Above for FPGA/CPLDS.

REFERENCE BOOKS:

1. Mixed Signal Laboratory Manual

M.Tech (VLSI) – II Semester
(14MT25721) MIXED SIGNAL LABORATORY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
25	50	75	-	-	4	2

PREREQUISITE:
A course on Circuit Level Design and Layouts

COURSE DESCRIPTION:
Design and verification of analog and mixed signal circuits.

COURSE OBJECTIVES:
CEO1: To acquire skills in design of Mixed Signal Designs and solve problems in layout design to enhance the quality of design for emerging technologies.

CEO2: To propose new techniques for development of ICs.

CE03: To provide opportunity to work with a strong sense of professionalism and code of engineering practice in CAD Tools suitable for industrial needs.

COURSE OUTCOMES: After the completion of the course, the student will be able to
CO1: Discriminate HDL Languages to model FPGA/ASIC design.

CO2: Conceptualize and solve problems in functional verification, timing and Power Analysis of Digital circuits.

CO3: Develop Skills to solve problems of layout design and build solutions for optimizing design for area, power and speed.

CO4: Conduct experiments for modeling devices suited for various communications.

CO5: Able to use CAD Tools to arrive at a optimized solution for mixed signal design.

CO6: Contribute positively to multidisciplinary scientific research in design and development of Mixed/Analog Integrated Circuits to solve problems arising in Integrated circuit Technology.

CO7: Perform projects efficiently in Digital system design to achieve optimization for high device utilization and performance in industrial needs.

DETAILED SYLLABUS:

Mentor Graphic tools / Cadence tools / Synopsis tools

1. **Backend Design** **(8 Slots)**

   Schematic Entry, Simulation, Layout, DRC, PEX, Post Layout Simulation of CMOS Logic Gates, Combinational Circuits (Adders, Encoders, Decoders, Multiplexers,

Demultiplexers, etc), Sequential Circuits(Flip Flops, Registers, counters), Biquad Filter, PLL and ADC/DAC.

2. Frontend/Semicustom Design (4 Slots)

HDL Design Entry, Logic Simulation, RTL Logic Synthesis, Post Synthesis Timing Simulation, Place & Route, Design for Testability, Static Timing Analysis, Power Analysis of Combinational and Sequential Circuits (Application Oriented designs – Traffic Light Controller, FSM based Control applications, etc).

Total Slots: 12

Required Software Tools:

1. Mentor Graphic tools / Cadence tools / Synopsis tools. (220 nm Technology and Above)
2. Xilinx ISE 10.1i and Above for FPGA/CPLDS.

REFERENCE BOOKS:

1. Mixed Signal Laboratory Manual

M.Tech. - II Semester
(16MT25732) NANOELECTRONICS LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	--	--	4	2

PRE-REQUISITES:
A course on Circuit Level Design

COUSRE DESCRIPTION:
Demonstration of the lab; Design, fabrication and verification of the nanoelectronic devices.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
    - Clean room,
    - Substrate preparation
    - Device fabrication
    - Device characterization
    - Device verification
2. Able to analyze
    - Nanostructure of the Devices
    - New material and Device characterization
3. Think laterally to get involved efficiently in research field of nanoelectronics.
4. Efficiently solve complex problem in the design of nanoelectronic devices.
5. Design and develop new nanodevice for advance technological application.
6. Use tools for verifying developed nanodevices.
7. Communicate effectively in verbal and written form for the experiments.
8. Utilize and implement the practical knowledge in multidiscipline areas.

LIST OF EXERCISES:

Demonstration, fabrication and characterization of nano devices (8 Slots)

1. Clean room demonstration
2. Clean bench demonstration
3. Demonstration of substrate
4. Cleaning of substrate
5. Deposition of filter by sol-gel method
6. Deposition of thermal evaporation
7. Device fabrication
8. Device characterization

Verification of fabricated devices (4 Slots)

9. Verification of device characteristics using MATLAB
10. Verification of device characteristics using COMSOL.

Total Time Slots: 12

REFERENCE BOOKS:

1. Nanoelectronics Lab Manual

M. Tech. – II Semester
(16MT23810) INTELLECTUAL PROPERTY RIGHTS
(Common to all M. Tech. Programs)
(Audit Course)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	-	2	-	-

PRE-REQUISITES: --

COURSE DESCRIPTION:

Introduction to Intellectual Property; Trade Marks; Law of Copy Rights; Law of Patents; Trade Secrets; Unfair Competition; New Development of Intellectual Property.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

1. Demonstrate in-depth knowledge on
   - Intellectual Property
   - Trade Marks & Secrets
   - Law of Copy Rights, Patents
   - New development of Intellectual Property
2. Analyze the different forms of infringement of intellectual property rights.
3. Solve problems pertaining to Intellectual Property Rights.
4. Stimulate research zeal for patenting of an idea or product.
5. Write effective reports required for filing patents.
6. Develop life-long learning capabilities.
7. Develop awareness of the relevance and impact of IP Law on their academic and professional lives.
8. Develop attitude for reflective learning.

DETAILED SYLLABUS:

UNIT - I: Introduction to Intellectual property (Periods:5)
Introduction, types of intellectual property, international organizations, agencies and treaties, importance of intellectual property rights.

UNIT - II: Trade Marks: (Periods:5)
Purpose and function of trademarks, acquisition of trade mark rights, protectable matter, selecting and evaluating trade mark, trade mark registration processes.

UNIT - III: Law of copy rights: (Periods:6)
Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.
Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer

UNIT - IV: Trade Secrets: (Periods:6)
Trade secrete law, determination of trade secrete status, liability for misappropriations of trade secrets, protection for submission, trade secrete litigation.

Unfair competition: Misappropriation right of publicity, False advertising.

UNIT - V: New development of intellectual property: (Periods:6)

New developments in trade mark law; copy right law, patent law, intellectual property audits.

International overview on intellectual property, international - trade mark law, copy right law, international patent law, international development in trade secrets law.

Total Periods: 28

REFERENCE BOOKS:

1. Deborah, E. Bouchoux, *Intellectual property right*, Cengage learning.
2. Prabuddha ganguli, *Intellectual property right - Unleashing the knowledge economy*, Tata Mc Graw Hill Publishing Company Ltd.