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TO,
Mr. Lakshmi Prasad B
Roll no: 18121D5702 (M Tech)
Sree vidhanikethan engineering College (SVEC)
Sree Sainath Nagar, Tirupathi - 517102

Dt. 10th May, 2019

Dear Lakshmi Prasad B,

Joining Date: 10th May 2019

Sub: Appointment as an INTERN.

Further to your above interview held in our office, the Management is pleased to welcome you to the family of M/s. BETA SCIENTIFICS as an **INTERN** and accordingly, this appointment order is issued to you. As an **INTERN** you are here to learn the advanced Technology of Physical Design, etc.
The following are the terms and conditions applicable to you.

1. You will be reporting to Mr. Narashima, Technical Head.
2. Your training period is for a period of 1 year from the date of your reporting to the company.
3. You will not be paid any kind of stipend.
4. You are required to learn the operations diligently and intelligently.
5. You are required to attend all classes, lectures, tests etc arranged by the management and submit reports for evaluation.
6. You are eligible for 1-day CL per month which accumulates.
7. You are governed by the rules and regulations of the company as applicable to the INTERNS in force and the amendments made from time to time.

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8. Contrary to the above said rules and regulations any action/ performance done by you like late coming, frequent leave taking, misuse of office equipment's, sharing the business secrets with outsiders etc will be treated as indiscipline and will be dealt accordingly.
9. You are required to maintain the up- keeping of all belongings of the office in good working conditions.
10. On successful completion of your Internship, Will be providing the Completion letter.
11. This contract is terminable by either side by giving one month's notice/one month's salary thereof. Interns absconding without giving proper notice and not returning the belongings of the company like mobile, charger, sim, earphone, laptop etc and training expenses, Management reserves the right to claim the amount towards the same against damages.

If you are agreeable to the above terms & conditions, sign and return the duplicate copy of this appointment order as a taken of your acceptance
With Best Wishes for your Successful Training.

Yours faithfully,

For BETA SCIENTIFICS
PROPRIETOR

Himabindu Kankata
HR Manager

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AN EXTENSIVE PROJECTION TO CREATE AN EFFICIENT CLOCK SPECIFICATIONS BASED ON DESIGN RULE VIOLATION CONSTRAINTS

A Project Report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANATAPUR, ANATAPURAMU

In partial fulfilment of the requirements

For the award of the degree of

MASTER OF TECHNOLOGY
IN
VLSI

Submitted by

B. LAKSHMI PRASAD (18121D5702)

Under the esteemed Guidance of

Mr. C. Venkata Sudhakar, M.Tech.,

Assistant professor, Dept. of ECE

Department of Electronics and Communication Engineering

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(Autonomous)

Sree Sainath Nagar, A.Rangampet, Tirupathi-517102

(2018 – 2020)

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To,

Dt. 10th May, 2019

Mr. Nagendra K
Roll no: 18121D5707 (M Tech)
Sree vidhanikethan engineering College (SVEC)
Sree Sainath Nagar, Tirupathi - 517102

Dear Nagendra K,

Joining Date: 10th May 2019
Sub: Appointment as an INTERN.

Further to your above interview held in our office, the Management is pleased to welcome you to the family of M/s. BETA SCIENTIFICS as an **INTERN** and accordingly, this appointment order is issued to you. As an **INTERN** you are here to learn the advanced Technology of Physical Design, etc.
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4. You are required to learn the operations diligently and intelligently.
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7. You are governed by the rules and regulations of the company as applicable to the INTERNS in force and the amendments made from time to time.

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8. Contrary to the above said rules and regulations any action/ performance done by you like late coming, frequent leave taking, misuse of office equipment's, sharing the business secrets with outsiders etc will be treated as indiscipline and will be dealt accordingly.
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If you are agreeable to the above terms & conditions, sign and return the duplicate copy of this appointment order as a taken of your acceptance
With Best Wishes for your Successful Training.

Yours faithfully,

For BETA SCIENTIFICS

PROPRIETOR

Himabindu Kankata
HR Manager

Scanned with CamScanner

Improved Algorithm to do Floorplan for Ultra ComplexSoC's

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
for the award of degree of

MASTER OF TECHNOLOGY
in
VLSI

Submitted by

K.NAGENDRA (18121D5707)

Under the Guidance of

Dr. N. ASHOK KUMAR,M. Tech.,(Ph. D),
Associate Professor, Dept. of ECE.

Department of Electronics and Communication Engineering

SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

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TO,

Dt. 10th May, 2019

Mr. Bhaskara P
Roll no: 18121D5713 (M Tech)
Sree vidhanikethan engineering College (SVEC)
Sree Sainath Nagar, Tirupathi - 517102

Dear Bhaskara P

Joining Date: 10th May 2019

Sub: Appointment as an INTERN.

Further to your above interview held in our office, the Management is pleased to welcome you to the family of M/s. BETA SCIENTIFICS as an **INTERN** and accordingly, this appointment order is issued to you. As an **INTERN** you are here to learn the advanced Technology of Physical Design, etc.
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2. Your training period is for a period of 1 Year from the date of your reporting to the company.
3. You will not be paid any kind of stipend.
4. You are required to learn the operations diligently and intelligently.
5. You are required to attend all classes, lectures, tests etc arranged by the management and submit reports for evaluation.
6. You are eligible for 1 day CL per month which accumulates.
7. You are governed by the rules and regulations of the company as applicable to the INTERNS in force and the amendments made from time to time.

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If you are agreeable to the above terms & conditions, sign and return the duplicate copy of this appointment order as a taken of your acceptance
With Best Wishes for your Successful Training.

Yours faithfully,

For BETA SCIENTIFICS
PROPRIETOR

Himabindu Kankata
HR Manager

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A Robust CTS algorithm using the H-Tree to minimize local skews of higher frequency targets of the SOC designs

A Project report submitted to

Jawaharlal Nehru Technological University Anantapur,

Anantapuramu

in partial fulfillment of the requirements
for the award of the degree of

Master of Technology
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Submitted by

BHASKARA PALAGANI
Roll No: 18121D5713

Under the esteemed guidance of

Mr. P.V.S.R. BHARADWAJA, M.Tech.,
Asst. Professor Department of ECE

Department of Electronics and Communication Engineering
SREE VIDYANIKETHAN ENGINEERING COLLEGE
(Autonomous)
Sree Sainath Nagar, Tirupathi – 517102.

(2018-2020)

Scalable Structures of Microprogrammed Digital Filter Using CSLA And Wallace Tree Multiplier

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
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MASTER OF TECHNOLOGY
in
VLSI

Submitted by

A. NIKHILA (18121D5701)

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Mr. M. NARESH BABU M. Tech., (Ph. D),
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SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

Characteristics & Performance Analysis of CNT based Field Effect Transistor for NEMS Considering Changes in Different Parameters

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
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MASTER OF TECHNOLOGY
in
VLSI

Submitted by

C. ASWINI (18121D5703)

Under the Guidance of

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SREE VIDYANIKETHAN ENGINEERING COLLEGE
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Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

Energy Efficient Single-Ended SRAM for Multimedia Applications

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
for the award of degree of

MASTER OF TECHNOLOGY
in
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Submitted by

DAKA SUNAYANA (18121D5704)

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T.Krishna Murthy, M.Tech.,(Ph.D.)
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SREE VIDYANIKETHAN ENGINEERING COLLEGE
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Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

Implementation of SoC SPARC Processor in 28nm Technology

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY
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Submitted by

Gudipati Pavan Kumar (18121D5705)

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Mr. P. MADHU KUMAR M. Tech., (Ph. D),
Assistant Professor, Dept. of ECE.

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SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)
Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

Design of an efficient CMOS rectifier for Energy harvesting applications

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements for the award of degree of

MASTER OF TECHNOLOGY
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Submitted by

J. HARITHA (18121D5706)

Under the Guidance of

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Professor, Department of ECE.

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Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

Very High Speed-Ultra Low Power CNTFET Magnitude Comparator Circuits

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAP
ANANTAPURAMU

in partial fulfillment of the requirements
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MASTER OF TECHNOLOGY
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Submitted by

Karanam.Haritha (18121D5708)

Under the Guidance of

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SREE VIDYANIKETHAN ENGINEERING COLLEGE
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Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

Image Encryption Using Ultra-Lightweight Block Cipher:PRESENT

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
for the award of degree of

MASTER OF TECHNOLOGY
in
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Submitted by

K.JOSHNAVANAJA (18121D5709)

Under the Guidance of

Mr.G.C.MADHU,M.Tech,(Ph.D),
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SREE VIDYANIKETHAN ENGINEERING COLLEGE
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Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

Design and Implementation of Router Architecture for High Performance Soft NoC

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
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in
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Submitted by

M.Sai Kumar (18121D5710)

Under the Guidance of

K.Neelima, M.Tech.,(Ph.D.)
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Department of Electronics and Communication Engineering

SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

Design of Double Edge Triggering Register Elements For Low Power And High Performance VLSI Clocking System

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
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MASTER OF TECHNOLOGY
in
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Submitted by

MANNEM POORNIMA (18121D5711)

Under the Guidance of

Dr. P. NAGARAJAN, M.E., Ph. D.,
Associate professor, Dept. of ECE.

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SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. Rangampet, Tirupathi - 517102.

(2018-2020)

High Speed Floating Point Multiply Accumulate Unit using Offset Binary Coding

A Project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
for the award of degree of

MASTER OF TECHNOLOGY
in
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Submitted by

P.L. LAHARI (18121D5712)

Under the Guidance of

Ms. M. Bharathi M. Tech., (Ph.D)
Assistant Professor, Dept. of ECE.

Department of Electronics and Communication Engineering

SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. Rangampet , Tirupathi - 517102.

(2018 - 2020)

Design and Optimization of ZnO Nanostructured SAW based Ethylene Gas Sensor with Modified Electrode Orientation

A project report submitted to

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR, ANANTAPURAMU

in partial fulfillment of the requirements
for the award of degree of

MASTER OF TECHNOLOGY
in
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Submitted by

T. JYOTHSNA (18121D5714)

Under the Guidance of

Ms.K.NEELIMA, M.Tech.,(Ph.D),
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Department of Electronics and Communication Engineering

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(2018-2020)