SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)

Sree Sainath Nagar, Tirupati

Department of Electronics and Communication Engineering

Supporting Document for 1.1.2

Syllabus Revision carried out in 2019

Program: M.Tech.- Digital Electronics and Communication Systems

Regulations : SVEC-19

This document details the following:

1. Courses where syllabus has been changed 20% and more.
2. Course-wise revised syllabus with changes highlighted.

Note: *For SVEC-19 revised syllabus, SVEC-16 (previous syllabus) is the reference.*

List of Courses where syllabus has been changed (20% and more)

Course Code	Name of the course	Percentage of Syllabus changed	Page Number in which Details are Highlighted
19MT13801	Advanced Digital Signal Processing	100	3
19MT15707	FPGA Architectures	70	5
19MT15708	Low Power CMOS VLSI Design	100	9
19MT13806	Adaptive Signal Processing	100	13
19MT13807	RF Circuit Design & Microwave Devices	100	15
19MT10708	Research Methodology and IPR	40	17
19MT13832	Communications and Signal Processing Lab	100	21
19MT1AC01	Technical Report Writing	100	23
19MT15706	VLSI Design Verification and Testing	20	25
19MT23802	MIMO System	100	29
19MT26305	Internet of Things	100	31
19MT23804	Software Defined Radio	100	33
19MT23831	Advanced Communications Lab	60	35
19MT23832	VLSI Design Verification and Testing Lab	100	39
19MT2AC01	Statistics with R	100	41
	Average	**86**	
	Total No. of Courses in the Program	28	
	No. of Courses where syllabus (more than 20%) has been changed	15	
	Percentage of Syllabus changed in the Program	**46.07**	

DEAN (Academics)
Dean (Academics)
Sree Vidyanikethan Engg. College
Sree Sainath Nagar
TIRUPATI - 517 102, A.P., India.

PRINCIPAL
PRINCIPAL
SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, A. RANGAMPET
Chittoor (Dist.) - 517 102, A.P., INDIA.

M.Tech. - I Semester
(19MT13801) ADVANCED DIGITAL SIGNAL PROCESSING
(Common to DECS & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Course on Digital Signal Processing at UG level

COURSE DESCRIPTION:

Digital filter banks; Parametric and Non-Parametric Power Spectrum Estimation methods; computationally efficient algorithms; Applications of DSP.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in Digital Signal Processing and applications
CEO2: To develop skills in design, analysis, problem solving and research in Multirate Signal Processing, Linear prediction, Power Spectral Estimation and Communications.

COURSE OUTCOMES:

After successful completion of the course, student will be able to:

CO1: Analyze sampling rate conversion, various DSP algorithms and design digital Filter Banks to improve performance characteristics of digital systems in multidisciplinary environments like image processing, wireless communication, biomedical engineering, speech processing, video processing, etc
CO2: Realize, compare and estimate power spectrum using different Non-Parametric and Parametric Methods in the frequency analysis of systems.
CO3: Understand Linear Prediction, analyze Lattice Forward and Backward Predictors for Radar signal Processing and Remote sensing.
CO4: Apply signal processing techniques in fields such as communications, speech processing, Image and video processing.

DETAILED SYLLABUS:

Unit-I: Multirate Filter Banks (Hours: 10)
Decimation, Interpolation, Sampling rate conversion by a rational factor I/D, Multistage Implementation of sampling rate conversion. **Digital Filter Banks**: Two-Channel Quadrature-Mirror Filter Bank, Elimination of aliasing, condition for Perfect Reconstruction, Polyphase form of QMF bank, Linear phase FIR QMF bank, IIR QMF bank, Perfect Reconstruction Two-Channel FIR QMF Bank.

Unit-II: DSP Algorithms (Hours: 08)
Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

Unit-III: Power Spectral Estimations (Hours: 09)

Estimation of spectra from finite duration observation of signals.

Non-Parametric Methods: Bartlett, Welch, Blackman & Tukey methods. Performance Characteristics of Non-parametric Power Spectrum Estimators, Computational Requirements of Non-parametric Power Spectrum Estimates.

Parametric Methods of Power Spectral Estimation:

Auto correlation & Its Properties, Relationship between auto correlation & model parameters, Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation.

Unit-IV: Linear Prediction (Hours: 08)

Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters.

Unit-V: Applications of Digital Signal Processing (Hours: 10)

Digital cellular mobile telephony, Adaptive telephone echo cancellation, High quality A/D conversion for digital Audio, Efficient D/A conversion in compact hi-fi systems, Acquisition of high quality data, Multirate narrow band digital filtering, High resolution narrow band spectral analysis.

Total Hours: 45

TEXT BOOKS:

1. John G. Proakis, Dimitris G. Manolakis, "*Digital signal processing, principles, Algorithms and applications",* Prentice Hall, 4th edition, 2007.
2. Sanjit K Mitra, "*Digital signal processing, A computer base approach",* McGraw-Hill Higher Education, 4th edition, 2011.

REFERENCE BOOKS:

1. Emmanuel C Ifeacher Barrie. W. Jervis, "*DSP-A Practical Approach*", Pearson Education, 2nd edition, 2002.
2. A.V. Oppenheim and R.W. Schaffer, "*Discrete Time Signal Processing",* PHI, 2nd edition, 2006.

M. Tech.– I Semester

(19MT15707) FPGA ARCHITECTURES

(Program Elective-2)

(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Digital Logic Design and VLSI Design at UG Level.

COURSE DESCRIPTION:

Evolution of Programmable Devices, Xilinx, Actel, Altera FPGAs, Logic Synthesis, Technology Mapping, Finite State Machines, Realizations of SM Charts, One Hot Method, System level Design, Device Applications-Fast Bus Controller, FIFO Controller & Intelligent I/O Subsystem

COURSE OBJECTIVES:

CEO1: To impart knowledge in architectures and applications of various families of CPLDs and FPGAs.
CEO2: To develop skills in design, analysis and problem solving for implementation and verification of functions in CPLDs/FPGAs.
CEO3: Apply knowledge and skills for performance analysis in the design of FSMs.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze the architectures of programmable logic devices and technology mapping issues in CPLDs and FPGAs.
CO2. Analyze various Finite state machine charts and its architectures to evaluate the performance of VLSI systems.
CO3. Understand the applications of FPGA in communications, speech processing, Image and video processing.

DETAILED SYLLABUS:

Unit - I: Introduction to Programmable Logic and FPGAs (Hours: 08)

Evolution of Programmable Devices, CPLD Altera Series Max 5000, MAX 7000 Series. Field Programmable Gate Arrays –Design Flow, Placement , Routing Architecture. Altera FPGAs. Advanced Micro Devices (AMD) FPGA. Applications of FPGAs.

Unit - II: (Hours: 09)

Xillinx and Actel FPGAs :

Case Studies – Xilinx XC2000, XilinxXC3000, Xilinx 4000 FPGAS. Actel FPGAs- Actel ACT1, Actel ACT2, Actel ACT3.

Technology Mapping for FPGAs: Logic Synthesis. Lookup Table Technology, Mapping Multiplexer Technology Mapping- The Proserphine Technology Mapper, Multiplexers Technology Mapping in Mis pga, A map and XA map Technology Mappers.

Unit - III: Finite State Machine (Hours: 09)

Finite State Machines, State Transition Table, State Assignment for FPGAs, Hazards and One Hot Encoding. Mustang. State Machine Charts, Derivations of State Machine Charges, Realization of State Machine Charts.

Unit - IV: FSM Architectures and System Level Design (Hours: 10)

Architectures Centered Around Non Registered PLDs, State Machine Designs Centered Around Shift Registers, One – Hot Design Method, Use of ASMs in One Hot Design, Application of One Hot Method. System Level Design – Controller, Data Path and Functional Partition.

Unit - V: Device Applications (Hours: 09)

MAX 5000 Timing, Using Expanders to Build Registered Logic in MAX EPLDs, Simulating Internal Buses in General Purpose EPLDs, Fast Bus Controllers with EPM5016, Micro Channel Bus Master and SDP Logic with the EPM5032 EPLD, FIFO Controller Using an EPM7096, Integrating an Intelligent I/O Subsystem with a Single EPM5130 EPLD.

Total Hours: 45

TEXT BOOKS:

1. S.Brown, R.Francis, J.Rose, Z.Vransic, "*Field Programmable Gate Array*", Kluwer Publication, 1992.
2. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall (PTE), 1994
3. Richard Tinder, "*Engineering Digital Design*", Academic Press, 2nd Edition, 2000.

REFERENCE BOOKS:

1. Charles H. Roth, Jr, "*Fundamentals of Logic Design*", Cengage Learning, 5th Edition, 2004.
2. S.Trimberger, Edr., "*Field Programmable Gate Array Technology*", Kluwer Academic Publications, 1994.

M. Tech. – I Semester
(16MT15707) FPGA ARCHITECTURES & APPLICATIONS
(PE - I)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PRE-REQUISITES:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
Fundamentals of Programmable devices; Logic Implementation using PLDs and FPGAs.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

1. Demonstrate advanced knowledge in
   - Programmable Logic Devices
   - Different FPGA Architectures
   - Digital Implementation using FPGA
   - FPGA Applications
2. Analyze complex problems critically for digital implementation issues, to conduct research in Digital VLSI Design.
3. Solve engineering problems with wide range of solutions in FPGA Implementation.
4. Initiate research methodologies in Modeling, Simulation and Implementation of complex engineering applications in the field of Digital Design at different levels of abstraction.
5. Apply appropriate techniques, Resources and tools in, Modeling complex engineering applications with an understanding of limitations.
6. Contribute to multidisciplinary scientific work in the field of FPGA Devices.

DETAILED SYLLABUS

UNIT–I: **Programmable logic Devices** **(Periods: 08)**
Programmable logic Devices: ROM, PLA, PAL, CPLD, FPGA Features, Architectures and Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT – II: FPGAs **(Periods: 12)**
Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs, Introduction to advanced FPGAs-Xilinx Virtex and ALTERA Stratix

UNIT -III: **(Periods: 14)**
Finite State Machines (FSM): Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.
FSM Architectures: Architectures centered around non registered PLDs, Design of state machines centered around shift registers, One Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.

UNIT – IV: System Level Design: **(Periods: 12)**
Controller, data path designing, Functional partition, Digital front end digital design tools for

FPGAs. System level design using mentor graphics/Xilinx EDA tool (FPGA Advantage/Xilinx ISE), Design flow using FPGAs.

UNIT – V: Case studies **(Periods: 09)**

Design considerations using FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers

Total periods: 55

TEXT BOOKS:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Kluwer Academic Publications, 1994.
2. Richard F. Tinder, "Engineering Digital Design", Academic Press, 2nd edition, 2000.
3. Charles H. Roth, "Fundamentals of logic design", Thomson/Brooks/Cole, 5th edition, 2004.

REFERENCE BOOKS:

1. Pak K. Chan & Samiha Mourad, "Digital Design Using Field Programmable Gate Array", PTR Prentice Hall, 1st edition, 1994.
2. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, "Field Programmable Gate Array", Kluwer Academic Publishers, 1st edition, 1992.

M. Tech. - I Semester
(19MT15708) LOW POWER CMOS VLSI DESIGN
(Program Elective - 2)
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on VLSI Design at UG Level

COURSE DESCRIPTION:

Need for low power VLSI chips, Sources of Power dissipation in MOS & CMOS Devices, Power Estimation, Synthesis of low power VLSI Circuits, Design of low power VLSI Circuits, Low power Memory Architectures, Energy recovery Circuits, Software design of low power VLSI Circuits.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in low power CMOS Circuits.
CEO2: To develop skills in design, analysis and problem solving related to high performance and low power devices.
CEO3: Apply knowledge and skills pertaining to low voltage CMOS circuit design for for wide range of IC applications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze the various power dissipation effects and estimation methods in CMOS VLSI Circuits to improve the performance characteristics of digital systems.
CO2. Understand the various design styles and synthesis of low power and low voltage CMOS VLSI circuits.
CO3. Analyze the various low power Static RAM architectures in design and development of Ultra Low power Integrated Circuits.
CO4. Apply energy recovery techniques to evaluate the performance of low power VLSI Circuits for scientific research in design and development of digital systems.

DETAILED SYLLABUS:

Unit –I **(Hours: 07)**
Power Dissipation in CMOS VLSI design: Need for low power VLSI chips, Sources of Power dissipation, Power dissipation in MOS & CMOS Devices, Limitations of low Power design.

Unit –II **(Hours: 08)**
Power Estimation: Modeling of Signals, Signal Probability Calculation, Probabilistic Techniques for Signal activity Estimation, Statistical Techniques, Estimation of Glitching

Power, Sensitivity Analysis, Power Estimation using input vector Compaction, Estimation of Maximum Power.

Unit-III **(Hours: 10)**

Synthesis for Low Power: Behavioral Level Transforms, Logic Level optimization of low power, Circuit level.

Design and Test of Low Voltage CMOS Circuits: Circuit Design Style, Leakage current in Deep Sub micrometer Transistors, Low voltage Circuit Design Techniques, Multiple Supply Voltages.

Unit-IV **(Hours: 10)**

Low Power Static RAM Architectures: Organization of Static RAM, MOS Static RAM Memory Cell, Banked Organization of SRAMs, Reducing Voltage Swing in Bit lines, Reducing Power in Sense Amplifier Circuits.

Unit-V **(Hours: 10)**

Low Energy Computing using Energy Recovery Techniques: Energy Recovery Circuit Design, Designs with partially Reversible logic, Supply Clock Generation.

Software design for low power: Sources of software power dissipation, software power estimation, Software power estimation, Co-design for low power.

Total Hours: 45

TEXT BOOK:

1. Kaushik Roy, Sharat Prasad, "*Low-Power CMOS VLSI Circuit Design*" Wiley Student Edition, 2000.

REFERENCE BOOK:

1. Kiat-Seng Yeo, Samir S.Rofail and Wang-Ling Goh, "*CMOS/BiCMOS ULSI: Low power, Low Voltage* ", Pearson education, 2002.

M. Tech. – II Semester
(16MT25701) LOW POWER VLSI DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:
A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:
Low Power Design Limitations; SOI and MOS/BICMOS Processes; Deep submicron processes; Integration/Isolation Considerations; CMOS/Bi-CMOS and Advanced Bi-CMOS Logic Gates; Design and Quality Measures of Low Power Latches & Flip-Flops; Special Low Power Techniques.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate in-depth knowledge in
    - Limitations of Low Power Design.
    - SOI Technology.
    - BiCMOS Processes.
    - MOSFET and BJT Behavior and Modeling.
    - BiCMOS Logic Gates Design.
    - Special low power techniques.
1. Analyze the low power BiCMOS circuits, the effects of devices and judge independently the best suited device for fabrication of smart devices for conducting research in ULSI design.
3. Solve problems of Low power design challenges, tradeoff between area, speed and power requirements.
4. Initiate research in low power VLSI design.
5. Apply appropriate techniques, resources and tools to engineering Activities in low power VLSI circuits.
6. Contribute to multidisciplinary scientific work in the field of low power Circuits.

DETAILED SYLLABUS:

UNIT –I: LOW POWER DESIGN AND AN OVER VIEW (Periods: 14)
Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.
MOS/BiCMOS Processes: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT –II: LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES (Periods: 11)
Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT-III: CMOS AND BI-CMOS LOGIC GATES (Periods: 12)
Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.
Low-Voltage Low-Power Logic Circuits: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS.

UNIT-IV: LOW POWER LATCHES AND FLIP FLOPS (Periods: 11)

Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT – V: SPECIAL TECHNIQUES (Periods: 07)

Power Reduction in Clock Networks, CMOS Floating Node,Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

Total Periods: 55

TEXT BOOKS:

1. Yeo Rofail/ Gohl (3 Authors), "CMOS/BiCMOS ULSI low voltage, low power", Pearson Education Asia, 1st Indian reprint, 2002.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCE BOOKS:

1. Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design", Prentice Hall, 3rd Illustrated Edition, 1994.
2. J. Rabaey, "Digital Integrated circuits: A Design perspective", Pearson Education, 2nd Edition, 2003.

M.Tech. - I Semester
(19MT13806) ADAPTIVE SIGNAL PROCESSING
(Common to DECS & CMS)
(Program Elective-2)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Signal Processing at UG Level

COURSE DESCRIPTION:

Development of adaptive filter theory; Method of steepest descent;Least-Mean-Square Algorithm and recursive least square algorithm; Kalman filtering algorithm; order -recursive adaptive filters.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in various adaptive algorithms for designing optimal filters.
CEO2: To analyze, design and implement adaptive filters using LMS, RLS and Kalman filtering algorithms for solving problems in the fields of signal processing, communications, Bio- Medical, Instrumentation and control engineering.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Understand linear optimum and adaptive filters to determine mean square error.
CO2: Analyze Steepest-Descent Algorithm and apply to the wiener filters.
CO3: Solve problems in the error minimization using LMS and RLS Algorithms.
CO4: Develop kalman and non Linear adaptive filters in the fields of signal processing, communications, Bio-Medical, Instrumentation and control engineering for optimization.
CO5: Analyze adaptive forward and backward linear prediction.

DETAILED SYLLABUS:

Unit-I: Introduction to Adaptive Systems & Development of Adaptive Filter Theory (Hours: 10)
Eigen Value Problem, Properties of eigen values and eigen vectors(proof is not required), Eigen Filters, eigen Value computations. The Filtering problem,Linear Optimum Filters, Adaptive Filters, Linear Filter sturucters, Approaches to the development of linear adaptive filters. Linear Optimum Filtering: Statement of the problem, Principle of Orthogonality, Minimum Mean Square Error, Wiener- Hopf equations, Error- Performance Surface.

Unit-II: Method of Steepest Descent (Hours: 07)
Basic Idea of Steepest-Descent Algorithm, Steepest-Descent Algorithm applied to the Wiener Filter, Stability of the Steepest-Descent Algorithm, Examination of the transient behavior of

the Steepest-Descent Algorithm, the Steepest-Descent Algorithm as a deterministic search method, Virtue and limitation of the Steepest-Descent Algorithm.

Unit-III: Least-Mean-Square Adaptive Filters and Recursive Least-Squares Adaptive Filters (Hours: 10)

Overview of the structure and operation of the Least-Mean-Square Algorithm, Least-Mean-Square adaptation Algorithm, Applications-Adaptive Noise cancelling Applied to a Sinusoidal Interference and Adaptive Beam forming, Comparison of the LMS Algorithm with Steepest-Descent Algorithm.

Matrix Inversion lemma, exponentially weighted recursive least square algorithm, update recursion for the sum of weighted error squares, Single-Weight Adaptive Noise Canceller convergence analysis of RLS Algorithm.

Unit-IV: Kalman Filtering & Non Linear Adaptive Filtering (Hours: 10)

Recursive Minimum Mean-Square Estimation for Scalar Random variables, Statement of Kalman filtering problem, The Innovations Process, estimation of the state using the Innovations Process, Filtering, Initial conditions.

An overview of the Blind Deconvolution problem, Buss Gang Algorithm for blind Equalization.

Unit-V: Order-Recursive Adaptive Filters (Hours: 08)

Gradient-Adaptive Lattice Filter, order-recursive adaptive filters using least square estimation, adaptive forward linear prediction, adaptive backward linear prediction, conversion factor, least-square lattice predictor, angle-normalized estimation errors, first order state space models for lattice filtering.

Total Hours: 45

TEXT BOOK:

1. Simon Haykin, *"Adaptive Filter Theory",* Pearson Education, 4th edition, 2002.

REFERENCE BOOK:

1. Bernard Widrow, Samuel D. Strearns, *"Adaptive Signal Processing",* Pearson Education, 1985.

M.Tech. - I Semester
(19MT13807) RF CIRCUIT DESIGN & MICROWAVE DEVICES
(Common to DECS & CMS)
(Program Elective-2)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Concept of Basic Electronics and Wave Theory at UG level

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in the fields of RF Circuits.
CEO2: To develop skills in analytical, problem solving, design and application skills in the broad area of RF circuit design.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Understand and apply the basic concepts of RF Electronics, analyze transmission lines, matching and biasing networks, and RF components, Design RF devices in Wireless Communications.
CO2: Realize, compare, and estimate problems in RF Passive and Active components as well as smart antenna techniques in the field of RF Circuits.
CO3: Analyze RF circuits and demonstrates use of Smith Chart for high frequency circuit design.
CO4: Apply techniques like MF-UHF for designing high-power microstrip circuits, directional couplers, transformers, composite and multilayer inductors, filters, combiners/dividers, and RFID systems in the field of wireless communication systems.
CO5: Analyze noise in RF devices like Oscillators, and synthesizers.

DETAILED SYLLABUS:

Unit-I: Introduction to RF Electronics (Hours: 09)
The Electromagnetic Spectrum, units and Physical Constants, Microwave bands, RF behavior of Passive components: Tuned resonant circuits, Vectors, Inductors and Capacitors. Voltage and Current in capacitor circuits, Tuned RF / IF Transformers.

Unit-II: Transmission Line Analysis (Hours: 12)
Examples of transmission lines, Transmission line equations and Biasing: Kirchoffs Voltage and current law representation, Traveling voltage and current waves, General Impedance definition, lossless transmission line model. Micro Strip Transmission Lines, Special Termination Conditions, sourced and Loaded Transmission Lines.
Single and Multiport Networks: The Smith Chart, Interconnectivity networks, Network properties and Applications, Scattering Parameters.

Unit-III: Microwave Components (Hours: 08)
Microwave resonators, Microwave filters, power dividers and directional couplers, Ferromagnetic devices and components.
Nonlinearity and Time Variance Inter-symbol interference, random process & noise, definition of sensitivity and dynamic range, conversion gain and distortion.

Unit-IV: Microwave Semiconductor Devices and Modeling (Hours: 08)
PIN diode, Tunnel diodes, Varactor diode, Schottky diode, IMPATT and TRAPATT devices, transferred electron devices, Microwave BJTs, GaAs FETs, low noise and power GaAs FETs, MESFET, MOSFET, HEMT.

Unit-V: Oscillators and Mixers (Hours: 08)
Oscillator basics, Low phase noise oscillator design, High frequency Oscillator configuration, LC Oscillators, VCOs, Crystal Oscillators, PLL Synthesizer, and Direct Digital Synthesizer.
RF Mixers: Basic characteristics of a mixer, Active mixers, Image Reject and Harmonic mixers, Frequency domain considerations.

Total Hours: 45

TEXT BOOKS:

1. Reinhold Ludwing, Pavel Bretchko, "*RF Circuit design: Theory and applications*", Pearson Education Asia Publication, 1st edition, New Delhi 2001.
2. D.M.Pozar, "*Microwave engineering*", Wiley, 4th edition, 2011.
3. Matthew M. Radmanesh, "*Advanced RF & Microwave Circuit Design: The Ultimate Guide to Superior Design*", Author House, 1st edition, 2009.

REFERENCE BOOKS:

1. Devendra K. Misra, "*Radio Frequency and Microwave Communication Circuits – Analysis and Design*", Wiley Student Edition, John Wiley & Sons, 2nd edition, July 2004.
2. Christopher Bowick, Cheryl Aljuni and John Biyler, "*RF Circuit Design*", Elsevier Science, 2nd edition, 2007.
3. S.Y. Liao, "*Microwave circuit Analysis and Amplifier Design*", Prentice Hall, 1st edition 1987.
4. Radmanesh, "*RF and Microwave Electronics Illustrated*", Pearson Education, 1st edition, 2004.

ADDITIONAL LEARNING RESOURCES

https://nptel.ac.in/courses/117102012/

M. Tech. - I Semester
(19MT10708) RESEARCH METHODOLOGY AND IPR

(Common to all M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	2	-	-	2

PRE REQUISITES:

COURSE DESCRIPTION:

Overview of research; research problem and design; various research designs; Data collection methods; Statistical methods for research;Interpretation& drafting reports and Intellectual property rights.

COURSE OBJECTIVES:

CEO1: To impart knowledge on research methodology and subsequent process involved for successful accomplishment of the research.
CEO2: To impart knowledge on intellectual property rights and subsequent process involved in filing patents and trade mark registration process.
CEO3: To inculcate attitude of reflective learning and contribute to the society through fruitful research.

COURSE OUTCOMES:

On successful completion of the course, students will be able to:

CO1. Apply the conceptual knowledge of research methodology to formulate the hypothesis, data collection and processing, analyzing the data using statistical methods, interpret the observations and communicating the novel findings through a research report.
CO2. Practice ethics and have responsibility towards society throughout the research process and indulge in continuous learning process.
CO3. Apply the conceptual knowledge of intellectual property rights for filing patents and trade mark registration process.

DETAILED SYLLABUS:

Unit-I: Introduction to Research Methodology (Hours: 07)
Objectives and Motivation of Research, Types of Research, Defining and Formulating the Research Problem; Features of research design, Different Research Designs; Different Methods of Data Collection, Data preparation and Processing.

Unit-II: Data Analysis and Hypothesis Testing (Hours: 09)
ANOVA; Principles of least squares-Regression and correlation; Normal Distribution-Properties of Normal Distribution; Testing of Hypothesis – Hypothesis Testing Procedure, Types of errors, t-Distribution, Chi-Square Test as a Test of Goodness of Fit.

Unit-III: Interpretation and Report Writing (Hours: 04)
Interpretation – Need, Techniques and Precautions; Report Writing – Significance, Different Steps, Layout, Types of reports,Mechanics of Writing a Research Report, Precautions in Writing Reports; Research ethics.

Unit-IV: Introduction to Intellectual property and Trade Marks (Hours: 07)
Importance of intellectual property rights; types of intellectual property, international organizations; Purpose and function of trademarks, acquisition of trade mark rights, protectable matter, selecting and evaluating trade mark, trade mark registration processes.

Unit-V: Law of Copyrights (Hours: 08)
Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.
Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer
New Developments in IPR: Administration of Patent System.

Total Hours: 35

TEXT BOOKS:

1. C.R. Kothari, *Research Methodology: Methods and Techniques*, 2nd revised edition, New Age International Publishers, New Delhi, 2004.
2. Deborah, E. Bouchoux, *Intellectual property right*, 5th edition, Cengage learning, 2017.

REFERENCE BOOKS:

1. R. Panneerselvam, *Research Methodology*, PHI learning Pvt. Ltd., 2009.
2. Prabuddha Ganguli, *Intellectual property right - Unleashing the knowledge economy*, Tata McGraw Hill Publishing Company Ltd, 2001.

M. Tech. – I Semester
(16MT13808) RESEARCH METHODOLOGY
(Common to all M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	-	2	-	-

PREREQUISITES: --

COURSE DESCRIPTION:

Overview of Research, research problem and design, various research designs, data collection methods, statistical methods for research, importance of research reports and its types.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Acquire in-depth knowledge on
   - Research design and conducting research
   - Various data collection methods
   - Statistical methods in research
   - Report writing techniques.
2. Analyze various research design issues for conducting research in core or allied areas.
3. Formulate solutions for engineering problems by conducting research effectively in the core or allied areas.
4. Carryout literature survey and apply research methodologies for the development of scientific/technological knowledge in one or more domains of engineering.
5. Select and Apply appropriate techniques and tools to complex engineering activities in their respective fields.
6. Write effective research reports.
7. Develop attitude for lifelong learning to do research.
8. Develop professional code of conduct and ethics of research.

DETAILED SYLLABUS:

Unit-I: Introduction to Research Methodology (Periods: 5)
Objectives and Motivation of Research, Types of Research, Research Approaches, Research Process, Criteria of good Research, Defining and Formulating the Research Problem, Problem Selection, Necessity of Defining the Problem, Techniques involved in Defining a Problem.

Unit-II: Research Problem Design and Data Collection Methods (Periods: 7)
Features of Good Design, Research Design Concepts, Different Research Designs, Different Methods of Data Collection, Data preparation: Processing Operations, Types of Analysis.

Unit-III: Statistics in Research (Periods:6)
Review of Statistical Techniques - Mean, Median, Mode, Geometric and Harmonic Mean, Standard Deviation, Measure of Asymmetry, ANOVA, Regression analysis.

Unit-IV: Hypothesis Testing (Periods: 7)

Normal Distribution, Properties of Normal Distribution, Basic Concepts of Testing of Hypothesis, Hypothesis Testing Procedure, Hypothesis Testing: t-Distribution, Chi-Square Test as a Test of Goodness of Fit.

Unit-V: Interpretation and Report Writing (Periods: 3)

Interpretation – Techniques and Precautions, Report Writing – Significance, Stages, Layout, Types of reports, Precautions in Writing Reports.

Total Periods: 28

TEXT BOOK:

1. C.R. Kothari, "*Research Methodology: Methods and Techniques*," New Age International Publishers, New Delhi, 2nd Revised Edition, 2004.

REFERENCE BOOKS:

1. Ranjit Kumar, "*Research Methodology: A step-by-step guide for beginners*," Sage South Asia, 3rd ed., 2011.
2. R. Panneerselvam, "Research Methodology," PHI learning Pvt. Ltd., 2009

M.Tech. - I Semester
(19MT13832) COMMUNICATIONS AND SIGNAL PROCESSING LAB
(Common to DECS & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

Simulation Lab at UG Level

COURSE DESCRIPTION:

Design and simulation of communication systems - QPSK communication system over AWGN channel and Rayleigh fading channel; Generation of maximal and Gold code sequences; Simulation of Rayleigh Fading Channel Using Either Clarke's Model or Jake's Model for different Doppler Spreads; Performance Evaluation of RAKE Receiver over Slow Fading Channel.

COURSE OBJECTIVES:

CEO1: To design, develop and simulate various components of digital communications and adaptive algorithms.
CEO2: To apply Knowledge and Skills to implement engineering Principles in the fields of Communications and Signal processing.

COURSE OUTCOMES:

On successful completion of this course the students will be able to

CO1: Analyze, measure, interpret and validate the practical observations by applying the conceptual knowledge of communication, signal and Image processing.
CO2: Design IIR and FIR filters for desired specifications.
CO3: Work individually and in groups to solve problems with effective communication.

LIST OF EXERCISES /EXPERIMENTS:

1. Design and Simulation FIR Filter Using any Windowing Technique.
2. Design of IIR Filters from Analog Filters.
3. Generation of Maximal Sequences and Gold Sequences.
4. Performance Evaluation of QPSK System over AWGN Channel.
5. Equalization of Multipath Channel using LMS or RLS Algorithms.
6. Simulation of Rayleigh Fading Channel Using Either Clarke's Model or Jake's Model for different Doppler Spreads (Ex. 50 Hz and 100 Hz).
7. Performance Evaluation of RAKE Receiver over Slow Fading Channel.
8. Performance Evaluation of QPSK System over Rayleigh Fading Channel.
9. Smoothening & Sharpening of a given image.
10. Color image in various color models.

REFERENCE BOOKS/LABORATORY MANUALS:

1. Communications and Signal Processing Lab Manual of the Department.
2. W.H. Tranter, K. Sam Shanmugham, T.S. Rappaport, and K.L. Kosbar, "*Principles of Communication System Simulation with Wireless Applications,"* Pearson, 2004.
3. J.G. Proakis, and M. Salehi, "*Contemporary Communication Systems using MATLAB and Simulink",* Cengage learning, 2nd edition, 2004.
4. R.C. Gonzalez, R. E. Woods, Steven L.Eddins, "*Digital Image Processing using MATLAB", Gatesmark Publishing*, 2nd edition, 2009.

M. Tech. - I Semester
(19MT1AC01) TECHNICAL REPORT WRITING
(Audit Course)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	*2*	-	-	-

PRE-REQUISITES: -

COURSE DESCRIPTION:

Introduction; Process of writing; Style of writing; Referencing; Presentation.

COURSE OBJECTIVES:

CEO1: To impart the knowledge of structure and layout of Business and Technical Reports.
CEO2: To learn styles and techniques of description for effective reports.
CEO3: To develop the ability to understand & interpret the writing techniques for effective communication in written documents.

COURSE OUTCOMES:

After successful completion of this course, the students will be able to:

CO1: Demonstrate knowledge of Technical Report Writing by examining kinds of reports and structure with scientific attitude.
CO2: Apply the techniques in preparing effective reports by examining Techniques of Description, Describing Machines and Mechanisms and Describing Processes.
CO3: Communicate effectively through writing technical reports by demonstrating the knowledge of Industry Reports, Survey Reports, Interpretive Report and Letter Report.

DETAILED SYLLABUS:

Unit I - **Introduction** **(Hours: 06)**
Introduction to Technical Report - Types of Reports - Planning Technical Report Writing - Components of a Technical Report - Report Writing in Science and Technology - Selecting and Preparing a 'Title' - Language Use in Report Writing.

Unit II - **Process of Writing** **(Hours: 05)**
Writing the 'Introduction' - Writing the 'Materials and Methods' - Writing the Findings/Results'- Writing the 'Discussion' - Preparing and using 'Tables'.

Unit III - **Style of Writing** **(Hours: 06)**
Preparing and using Effective 'Graphs' - Citing and Arranging References—I - Citing and Arranging References —II - Writing for Publication in a Scientific Journal.

Unit IV - **Referencing** **(Hours: 09)**
Literature citations - Introductory remarks on literature citations - Reasons for literature citations – Bibliographical data according to ISO - Citations in the text - Copyright and copyright laws - The text of the Technical Report - Using word processing and desktop

publishing (DTP) systems - Document or page layout and hints on editing - Typographic details - Cross-references.

Unit V - **Presentation** **(Hours: 04)**

Giving the presentation - Appropriate pointing - Dealing with intermediate questions - Review and analysis of the presentation - Rhetoric tips from A to Z.

Total Hours: 30

TEXT BOOKS:

1. R C Sharma – Krishna Mohan, *"Business Correspondence and Report Writing,"* Tata McGraw-Hill Publishing Company Limited, New Delhi, Third Edition, 2005 (reprint).
2. Patrick Forsyth*, "How to Write Reports and Proposals",* THE SUNDAY TIMES (Kogan Page), New Delhi, Revised Second Edition, 2010.

REFERENCE BOOKS:

1. John Seely, "*The Oxford Writing & Speaking"*, Oxford University Press, Indian Edition.
2. Anne Eisenberg, "*A Beginner's Guide to Technical Communication"*, McGraw Hill Education (India) Private Limited, New Delhi, 2013.

ADDITIONAL LEARNING RESOURCES

1. http://www.resumania.com/arcindex.html
2. http://www.aresearchguide.com/writing-a-technical-report.html
3. http://www.sussex.ac.uk/ei/internal/forstudents/engineeringdesign/studyguides/techreportwriting

M. Tech. - I/II Semester
(19MT15706) VLSI DESIGN VERIFICATION AND TESTING
(Program Elecive-1)
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Courses on VLSI Design, Digital IC Applications at UG Level.

COURSE OBJECTIVES:

CEO1: To impart in-depth knowledge in generation of test vectors for digital systems.
CEO2: To analyze and test the various faults in digital system design and develop fault free applications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze Modeling of Digital Circuits at various levels of abstraction and various types of logic Simulations.
CO2. Understand the various fault models, reduction techniques to apply for fault sampling and simulation.
CO3. Apply the automatic test generation techniques for testing Single Stuck at Faults and bridging faults in digital circuits.
CO4. Analyze the various testing approaches and Built-In Self Test architectures for testing digital circuits.

DETAILED SYLLABUS:

Unit –I: Introduction to Testing (Hours: 08)
Modeling-Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

Unit–II: Fault Modeling and Simulation (Hours: 09)
Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, Fault Simulation Techniques, Fault Sampling.

Unit-III: Testing for Stuck Faults (Hours: 09)
ATG for SSFs in Combinational Circuits and Sequential Circuits, Detection of Non feedback and Feedback Bridging Faults.

Unit–IV: Design for Testability (Hours: 09)
Controllability and Observability, Scan-Based Designs and Architecture, Board-Level and System-Level DFT Approaches, Compression Techniques, Syndrome Testing and Signature Analysis.

Unit-V: Built-In Self Test **(Hours: 10)**

Introduction to BIST Concepts, Test - Pattern Generation, off-line BIST Architectures, Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO.

Total Hours: 45

TEXT BOOK:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, *"Digital Systems Testing and Testable Design",* Wiley, 1st Edition, 1994.

REFERENCE BOOKS:

1. Alfred L. Crouch, "*Design for Test for Digital ICs & Embedded Core Systems",* Prentice Hall PTR, 1st Reprint Edition, 1999.
2. Robert J.Feugate, Jr., Steven M.McIntyre, "*Introduction to VLSI Testing*", Prentice Hall, 1st Illustrated Edition, 1998.

ADDITIONAL LEARNING RESOURCES

http://www2.eng.cam.ac.uk/~dmh/4b7/resource/section16.htm

https://nptel.ac.in/courses/106103016/21

https://nptel.ac.in/courses/106105161/54

M. Tech. - II Semester
(16MT25705) TESTING AND TESTABILITY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	4	-	-	4

PREREQUISITE:
A Course on Digital Logic Design at UG Level.

COURSE DESCRIPTION:
Design for testability; Fault modeling and simulation; Test analysis for digital circuits; Design strategies for testability.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonstrate advanced knowledge in
   - The basic faults that occur in digital systems
   - Testing of stuck at faults for digital circuits
   - Design for testability
2. Analyze testing issues in the field of digital system design critically for Conducting Research.
3. Solve engineering problems by modeling different faults for fault free Simulation in Digital circuits.
4. Apply appropriate research methodologies to develop New testing Strategies for digital and mixed signal circuits and systems.
5. Apply appropriate techniques, Resources and tools in, Modeling to Complex Engineering activities with an understanding of the limitations.
6. Contribute to multidisciplinary scientific work in the field of testing of Stuck at Faults for digital circuits.

DETAILED SYLLABUS:

UNIT –I: INTRODUTION TO TEST AND DESIGN FOR TESTABILITY (Periods: 13)
Modeling-Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT–II: FAULT MODELLING (Periods: 09)
Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, the Single Stuck-Fault Model, The Multiple Stuck-Fault Model.

UNIT-III: FAULT SIMULATION (Periods: 07)
Applications, General Fault Simulation Techniques, Fault Simulation for Combinational Circuits, Fault Sampling.

UNIT-IV: TESTING FOR SINGLE STUCK FAULTS (Periods: 12)
ATG for SSSFs in Combinational Circuits and Sequential Circuits, Testing for bridging faults, Functional Testing With Specific Fault Models, Vector Simulation- ATPG Vectors, Formats Compaction and Compression, Selecting ATPG Tool.

UNIT–V: DESIGN FOR TESTABILITY (Periods: 14)
Testability Trade Offs, Techniques, Scan Architectures and Testing, Controllability and Observability by means of Scan Registers, Generic Scan-Based Designs, Full Serial

Integrated Scan, Storage Cells for Scan Designs, Board-Level and System-Level DFT Approaches, Boundary Scans Standards, Compression Techniques, Different Techniques, Syndrome Testing and Signature Analysis, Introduction to BIST Concepts.

Total periods: 55

TEXT BOOKS:

3. MironAbramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Wiley, 1st Edition, 1994.
4. Alfred L. Crouch, "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall PTR, 1st Reprint Edition, 1999.

REFERENCE BOOK:

1. Robert J.Feugate, Jr., Steven M.Mclntyre, "Introduction to VLSI Testing", Prentice Hall, 1st Illustrated Edition,1998.

M.Tech. - II Semester
(19MT23802) MIMO SYSTEM
(Common to DECS & CMS)
(Program Elective-3)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Concept of Basic Electronics and Wave Theory at UG level

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in the fields of MIMO.
CEO2: To develop analytical, problem solving, design and application skills in the broad area of MIMO System.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Understand multi-antenna systems, channel modeling and effect of LOS and XPD on MIMO Capacity.
CO2: Analyze diversity and spatial multiplexing in MIMO systems.
CO3: Apply MIMO coding techniques in the field of wireless communication systems.

DETAILED SYLLABUS:

Unit-I: Introduction to MIMO System (Hours: 06)

Introduction to Multi-antenna Systems, Motivation, Types of multi-antenna systems, MIMO vs. multi-antenna systems.

Unit-II: The MIMO Wireless Channel (Hours: 10)

Introduction, preliminaries, MIMO System Model, MIMO System Capacity, Channel Unknown to the Transmitter, Channel known to the Transmitter, Deterministic Channel, Random Channels, Influence of Fading Correlation on MIMO Capacity, Influence of LOS on MIMO Capacity, Influence of XPD on MIMO Capacity, Keyhole Effect: Degenerate Channels, Capacity of Frequency Selective MIMO Channels.

Unit-III: MIMO Diversity and Spatial Multiplexing (Hours: 09)

Sources and types of diversity, analysis under Rayleigh fading, Diversity and channel knowledge. Alamouti space time code, MIMO spatial multiplexing. Space time receivers. ML, ZF, MMSE and Sphere decoding, BLAST receivers and Diversity multiplexing trade-off.

Unit-IV: Space Time Block Codes (Hours: 10)

Space time block codes on real and complex orthogonal designs, Code design criteria for quasistatic channels (Rank, determinant and Euclidean distance), Orthogonal designs, Generalized orthogonal designs, Quasi-orthogonal designs and Performance analysis.

Unit-V: Space Time Trellis Codes (Hours: 10)

Representation of STTC, shift register, generator matrix, state-transition diagram, trellis diagram, Code construction, Delay diversity as a special case of STTC and Performance analysis.

Total Hours: 45

TEXT BOOKS:

T1. Claude Oestges, Bruno Clerckx, "*MIMO Wireless Communications: From Real-world Propagation to Space-time Code Design*", Academic Press, 1st edition, 2010.

T2. Mohinder Janakiraman, "*Space-Time Codes and MIMO Systems*", Artech House Publishers, 1st edition 2004.

REFERENCE BOOKS:

R1. David Tse and Pramod Viswanath, "*Fundamentals of Wireless Communication*", Cambridge University Press, 1st edition, 2005.

R2. Paulraj, R. Nabar and D. Gore, "*Introduction to Space-Time Wireless Communications*", Cambridge University Press, 1st edition, 2003

R3. E.G. Larsson and P. Stoica, "*Space-Time Block Coding for Wireless Communications*", Cambridge University Press 1st edition, 2008.

ADDITIONAL LEARNING RESOURCES

www.sabre.org, www.bookaid.org, NPTEL

M.Tech. - II Semester
(19MT26305) INTERNET OF THINGS
(Common to CNIS, CS, SE, DECS and CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Computer Networks, Python Programming.

COURSE DESCRIPTION:

Concepts of Domain Specific IoTs, M2M and system management with Netconf-Yang, IoT privacy and security, IoT physical devices, Amazon Web Services for IoT and case studies illustrating IoT design.

COURSE OUTCOMES:

CO1: Understand the concepts of IoT, IoT protocols, privacy and security issues in IoT applications to analyze domain specific IoT's.
CO2: Design solutions through implementing IoT applications on raspberry pi, AWS and develop security solutions to strengthen IoT environment.

DETAILED SYLLABUS:

Unit-I: Concepts of IoT (Hours: 07)
Definition and characteristics of IoT, Physical design of IoT – IoT protocols, Logical design of IoT, IoT enabling technologies, IoT levels and deployment templates.

Unit-II: Domain Specific IoTs & IoT and M2M (Hours: 09)
Domain Specific IoTs: Home automation, Cities, Environment, Energy, Logistics, Agriculture, Industry.
IoT and M2M: Introduction, M2M, Difference between IoT and M2M, SDN and NFV for IoT.

Unit-III: IoT System Management with Netconf-Yang and Developing Internet of Things (Hours: 09)
Need for IoT systems management, Simple Network Management Protocol (SNMP), Network operator requirements, NETCONF-YANG, IoT systems management with NETCONF-YANG.
Developing Internet of Things: Introduction, IoT design methodology.

Unit-IV: IoT Privacy, Security and Vulnerabilities Solutions and IoT Physical Devices (Hours: 11)
Introduction, Vulnerabilities, Security requirements and treat analysis, Use cases and misuse cases, IoT security tomography and layered attacker model, Identity management and establishment, Access control and secure message communication, Security models, Profiles and protocols for IoT.
IoT Physical Devices & Endpoints: What is an IoT device, Exemplary device, About the board, Linux on Raspberry Pi, Raspberry Pi interfaces, Programming Raspberry Pi with Python and other IoT devices.

Unit-V: Amazon Web Services for IoT and Case Studies Illustrating IoT Design (Hours: 09)

Amazon Web Services for IoT: Amazon EC2, Amazon AutoScaling, Amazon S3, Amazon RDS, Amazon DynamoDB.

Case Studies Illustrating IoT Design: Home automation, Cities, Environment and Agriculture.

Total Hours: 45

TEXT BOOKS:

1. Arshdeep Bahga, Vijay Madisetti, "*Internet of Things: A Hands-on Approach"*, Universities Press, 2015.
2. Raj Kamal, "*Internet of Things: Architecture and Design Principles*", McGraw Hill, 1st Edition, 2017.

REFERENCE BOOKS:

1. Adrian McEwen, Hakim Cassimally, "*Designing the Internet of Things"*, Wiley, 2013.
2. Jeeva Jose, "*Internet of Things"*, Khanna Publishing, 1st Edition, 2018.

M.Tech. - II Semester
(19MT23804) SOFTWARE DEFINED RADIO
(Common to DECS & CMS)
(Program Elective-4)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PREREQUISITES:

A Course on Wireless Communication, Digital Signal Processing and Antennas at UG Level.

COURSE DESCRIPTION:

Principles of software defined radio; Multirate digital filter banks; Analysis and Synthesis of signals performance; Smart antennas with applications.

COURSE OBJECTIVES:

CEO1. To provide advanced knowledge in various aspects of Software Defined Radio.
CEO2. To impart analysis, problem solving, design, simulation, Interdisciplinary, Communication and application skills in Software Defined Radio.
CEO3. To imbibe ethical attitude towards environment and society.

COURSE OUTCOMES:

After successful completion of this course the students will be able to

CO1. Understand Radio frequency Implementation issues in software defined radios.
CO2. Design multirate digital filters for multirate signal processing for digital frequency converters in digital receivers.
CO3. Analyze the performance of direct digital synthesis systems in designing software defined radios.
CO4. Apply appropriate techniques for hardware implementation of smart antennas using software radio for better spectrum exploitation.
CO5. Analyze a Software defined Radio System/ Subsystem with object oriented representation for public needs.

DETAILED SYLLABUS:

Unit-I: Introduction to Software Radio Concepts (Hours: 09)
The need for Software radios and its definition, Characteristics and benefits of Software radio, Design principles of a software radio.
Radio Frequency Implementation Issues: Purpose of RF front – end,Dynamic range, RF receiver front – end topologies, Enhanced flexibility of the RF chain with software radios, Importance of the components to overall performance, Transmitter architectures and their issues, Noise and distortion in the RF chain, ADC & DAC distortion, Pre-distortion, Flexible RF systems using micro-electromechanical systems.

Unit-II: Multirate Signal Processing in SDR (Hours: 09)
Sample rate conversion principles, Polyphase filters, Digital filter banks, Timing recovery in

digital receivers using multirate digital filters.
Digital Frequency Up-and Down Converters- Introduction- Frequency Converter Fundamentals- Digital NCO- Digital Mixers- Digital Filters- Half band Filters- CIC Filters- Decimation, Interpolation, and Multirate Processing-DUCs - Cascading Digital Converters and Digital Frequency Converters.

Unit-III: Digital Generation of Signals (Hours: 09)
Introduction, Comparison of direct digital synthesis with analog signal synthesis, Approaches to direct digital synthesis, Analysis of spurious signals, Spurious components due to periodic jitter, Band pass signal generation, Performance of direct digital synthesis systems, Hybrid DDS – PLL Systems, Applications of direct digital synthesis, Generation of random sequences, ROM compression techniques.

Unit-IV: Smart Antennas using Software Radio (Hours: 09)
Introduction, Vector channel modeling, Benefits of smart antennas, Structures for beam forming systems, Smart antenna algorithms, Diversity and Space time adaptive signal processing, Algorithms for transmit STAP, Hardware implementation of smart antennas, Array calibration, Digital Hardware Choices-Key hardware elements, DSP processors, FPGAs, Power management issues. Applying Software Radio Principles to Antenna Systems-Smart Antenna Architectures- Optimum Combining/ Adaptive Arrays- DOA Arrays- Beam Forming for CDMA- Downlink Beam Forming.

Unit-V: Object Oriented Representation of Radios and Network (Hours: 09)
Networks, Object –oriented programming, Object brokers, Mobile application environments, Joint Tactical radio system.
Case Studies in Software Radio Design: SPEAKeasy, JTRS, Wireless Information transfer system, SDR-3000 digital transceiver subsystem, Spectrum Ware, Brief introduction to Cognitive Networking.

Total Hours: 45

TEXT BOOKS:

1. Jeffrey Hugh Reed, "*Software Radio: A Modern Approach to Radio Engineering*", Prentice Hall Professional, 2002.
2. Paul Burns, "*Software Defined Radio for 3G*", Artech House, 2002.

REFERENCE BOOKS:

1. Tony J Rouphael, "*RF and DSP for SDR*", Elsevier Newnes Press, 2008.
2. P. Kenington, "*RF and Baseband Techniques for Software Defined Radio*", Artech House, 2005.
3. Paul Burns, "*Software Defined Radio for 3G*", Artech House, 2002.
4. Tony J Rouphael, "*RF and DSP for SDR*", Elsevier Newnes Press, 2008.
5. JoukoVanakka, "*Digital Synthesizers and Transmitter for Software Radio*", Springer, 2005.
6. P Kenington, "*RF and Baseband Techniques for Software Defined Radio*", Artech House, 2005.

M.Tech. - II Semester
(19MT23831) ADVANCED COMMUNICATIONS LAB
(Common to DECS & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

Simulation lab at UG level

COURSE DESCRIPTION:

Simulation of communication systems over communication channels with and without line coding; Design and simulation of Bussgang Blind channel; Minimum Mean Square Error and zero force equalizer; Adaptive equalizers using LMS and RLS algorithms.

COURSE OBJECTIVES:

CEO1: To design, develop and simulate various components of communication System and adaptive equalizers.
CEO2: To apply knowledge and skills in implementation of engineering principles in the field of Communications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to

CO1: Analyze , measure, interpret and validate the practical observations by applying the conceptual knowledge of digital communications and adaptive signal processing.
CO2: Design CDMA communication system over different channels with Various adaptive equalizers for desired specifications.
CO3: Work individually and in groups to solve problems with effective communication.

LIST OF EXERCISES /EXPERIMENTS:

1. Design and simulation of M-ary QAM system with AWGN fading channel.
2. Simulation of Rayleigh fading channel in the mobile environment.
3. Design and performance evaluation of CDMA communication system over a Gaussian channel.
4. Design and performance evaluation of CDMA communication system over a multipath Rayleigh fading channel.
5. Simulation of communication system using convolutional codes & Viterbi Decoding.
6. Design and simulation of an adaptive equalizer using LMS algorithm.
7. Design and simulation of an adaptive equalizer using RLS algorithm.
8. Design and simulation of communication system using Bussgang Blind channel equalizer.
9. BER evaluation for BPSK modulation system with Minimum Mean Square Error (MMSE) equalization in 3 tap ISI channel.
10. BER evaluation for BPSK modulation system with Zero force Equalization in 3 tap ISI channel.

REFERENCE BOOKS/LABORATORY MANUALS:

1. Advanced communication lab manual of the department.
2. W.H. Tranter, K. Sam Shanmugham, T.S. Rappaport, and K.L. Kosbar, "*Principles of Communication System Simulation with Wireless Applications",* Pearson, 2004.
3. J.G. Proakis, and M. Salehi, "*Contemporary Communication Systems using MATLAB",* cengage learning, *2nd Edition,* 2004.

SOFTWARES/TOOLS USED:

MATLAB with communication and Signal Processing tool boxes.

M. Tech. - II SEMESTER
(16MT23831) COMMUNICATIONS LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

RE-REQUISITES: Simulation Lab at UG Level

COURSE DESCRIPTION:
Design and simulation of communication systems - QPSK communication system over AWGN channel, Baseband Direct Sequence Spread Spectrum (DS/SS) System; Generation of different density and distribution functions; Generation of maximal and Gold code sequences.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
1. Demonsrate Knowledge in
   - Generation of Maximal and Gold Sequences & verification of their properties.
   - Design of communication system for band limited channels for Zero ISI.
   - Evaluating the performance of QPSK over AWGN Channel and Rayleigh Fading Channels.
   - Simulation of Code matched filter in Spread Spectrum Communication System.
   - Simulation of baseband Direct Sequence Spread Spectrum (DS/SS) System.
   - Performance evaluation of RAKE Receiver over Slow Fading Channel.
   - Simulation of Rayleigh Fading Channel Using Either Clarke's Model or Jake's Model for different Doppler Spreads.
2. Analyze engineering problems for feasible and optimal solutions in the core area of communication.
3. Design of Matched filter for spread spectrum communications.
4. Use MATLAB Toolbox to simulate complex engineering activities in the field of communication.
5. Demonstrate knowledge and understanding of engineering principles to execute the Projects effectively in the field of communications.

LIST OF EXERCISES:
1. Generation of discrete time independent and identically distributed (IID) random processes with different distributions (Bernoulli, Binomial, Geometric, Poisson, Uniform, Gaussian, Exponential, Laplacian, Rayleigh, Rician). (1 time slot)
2. Communication system Design for Band limited Channels: System design for Zero ISI. (2 time slots)
3. Equalization of Multipath Channel using LMS or RLS Algorithms. (1 time slot)
4. Performance Evaluation QPSK communication system over AWGN channel. (1 time slot)
5. Generation of Maximal sequences & Gold codes and verification of their correlation properties. (2 time slots)
6. Design and simulation of code matched filter in spread spectrum communication system. (1 time slot)
7. Design and simulation of baseband Direct Sequence Spread Spectrum (DS/SS) System. (1 time slot)
8. Simulation of Rayleigh Fading Channel Using Either Clarke's Model or Jake's Model for different Doppler Spreads (Ex. 50 Hz and 100 Hz). (2 time slots)
9. Performance Evaluation of RAKE Receiver over Slow Fading Channel.

(2 time slots)

10. Performance Evaluation of QPSK System over Rayleigh Fading Channel.

(1 time slots)

Total Time Slots: 14

Tools:

Numerical Computing Environments–GNU Octave or MATLAB or any other equivalent tool

REFERENCE BOOKS:

1. W.H. Tranter, K. Sam Shanmugham, T.S. Rappaport, and K.L. Kosbar, *Principles of Communication System Simulation with Wireless Applications,* Pearson, 2004.
2. J.G. Proakis, and M. Salehi, *Contemporary Communication Systems using MATLAB,* Book ware Companion Series, 2006.
3. John G. Proakis, "DIGITAL COMMUNICATIONS", McGraw Hill, 4th edition, 2001.

M.Tech. - II Semester
(19MT23832) VLSI DESIGN VERIFICATION AND TESTING LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PREREQUISITES:

Course on VLSI Design Verification and Testing.

COURSE DESCRIPTION:

Modeling in HDL, Testing Single and Multiple Stuck at Faults, Testing Bridging Faults, Assessing Controllability and Observability, Test Vector Generation and Compression, BIST.

COURSE OBJECTIVES:

CEO1: To impart knowledge on modeling faults in combinational and sequential circuits.
CEO2: To develop and apply algorithms for testing the digital systems.
CEO3: To develop programming skills to solve problems in assessing fault coverage of developed designs.

COURSE OUTCOMES:

After successful completion of the course, students will be able to

CO1: Demonstrate hands-on experience on modeling faults for digital circuits and estimation of fault coverage and related parameters.
CO2: Develop test generation and test compression algorithms.
CO3: Apply developed algorithms to estimate required parameters for reducing the test time, storage requirements, etc.
CO4: Work individually and in groups to solve problems with effective communication.

LIST OF EXERCISES /EXPERIMENTS: (10-12 Exercises/Experiments)

1. Model a given Boolean Equation or Combinational Logic Design using Hardware Description Language and Assess the Parameters like Area, Delay and Power.

2. Model a given Boolean Equation or Sequential Logic Design using Hardware Description Language and Assess the Parameters like Area, Delay and Power.

3. Model Single Struck at Fault in a given Digital Circuit using Hardware Description Language and Verify it by using
   (i) D – algorithm and
   (ii) PODEM Algorithm

4. Model Multiple Struct at Fault in a given Digital Circuit using Hardware Description Language and develop test vectors that can detect every Single Stuck at Fault but not the Multiple Stuck at Faults.

5. Model Feedback and Non - Feedback Bridging Fault in a given Digital Circuit using

Hardware Description Language and develop test vectors that can detect it.

6. Design a Linear Feedback Shift Register and Model it using Hardware Description Language to develop test vectors.

7. Design a Pseudo Random Pattern Generator and Model it using Hardware Description Language to develop test vectors.

8. Model SCOPA Algorithm using Hardware Description Language to obtain Observability and Controllability of each node in the given logic circuit.

9. Model the Partial and Full Scan based Testing using Hardware Description Language and Assess the test methods based on test time, storage, etc.

10. Design a Signature Analysis based on Cyclic Redundancy Checking to generate test vectors by modeling in Hardware Description Language.

11. Develop a Memory Built In Self Test Architecture, model it by using Hardware Description Language and Verify it for various Modes of Operation.

12. Model Compression Techniques based on ones count, transition count, Parity check by using Hardware Description Language and verify its functionality.

13. Mini Projects (MPs):
    Form a group of maximum 2 members as a team and assign mini projects related to Testing of SoC or NoC based applications.

REFERENCE BOOKS/LABORATORY MANUALS:

1. ECE Department Lab Manual on VLSI Design Verification and Testing
2. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Wiley, 1st Edition, 1994.

SOFTWARES/TOOLS USED:

Cadence/ Synopsys/ Mentor Graphics Tools

ADDITIONAL LEARNING RESOURCES

https://www.iitg.ac.in/cseweb/vlab/vlsi/

M. Tech. – II Semester
(19MT2AC01) STATISTICS WITH R
(Audit Course)
(Common to All M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	2	-	-	-

PRE-REQUISITES: A course on Statistics.

COURSE DESCRIPTION:
Concepts of R programming basics, Bivariate and multivariate data, Confidence intervals, Goodness of fit, Analysis of variance.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
CO1: Import, manage, manipulate, and structure data files using R programming.
CO2: Implement models for statistical analysis of a given dataset and visualize the results to identify trends, patterns and outliers in data.

DETAILED SYLLABUS:

UNIT I - INTRODUCTION (Hours : 05)
Data, R's command line, Variables, Functions, The workspace, External packages, Data sets, Data vectors, Functions, Numeric summaries, Categorical data.

Unit II - BIVARIATE AND MULTIVARIATE DATA (Hours : 07)
Lists, Data frames, Paired data, Correlation, Trends, Transformations, Bivariate categorical data, Measures of association, Two-way tables, Marginal distributions, Conditional distributions, Graphical summaries, Multivariate data - Data frames, Applying a function over a collection, Using external data, Lattice graphics, Grouping, Statistical transformations.

UNIT III - POPULATIONS (Hours : 06)
Populations, Discrete random variables, Random values generation, Sampling, Families of distributions, Central limit theorem, Statistical Inference - Significance tests, Estimation, Confidence intervals, Bayesian analysis.

UNIT IV - CONFIDENCE INTERVALS (Hours : 06)
Confidence intervals for a population proportion, *p* - population mean, Other confidence intervals, Confidence intervals for differences, Confidence intervals for the median, Significance test - Significance test for a population proportion, Significance test for the mean (t-tests), Significance tests and confidence intervals, Significance tests for the median.

UNIT V - GOODNESS OF FIT (Hours : 06)
The chi-squared goodness-of-fit test, The multinomial distribution, Pearson's χ^2-statistic, chi-squared test of independence and homogeneity, Goodness-of-fit tests for continuous distributions, ANOVA - One-way ANOVA, Using *lm* for ANOVA.

Total Hours: 30

TEXT BOOKS:

1. John Verzani, *Using R for Introductory Statistics*, CRC Press, 2nd Edition, 2014.
2. Sudha G Purohit, Sharad D Gore, Shailaja R Deshmukh, *Statistics Using R*, Narosa Publishing house, 2nd Edition, 2015.

REFERENCE BOOKS:

1. Francisco Juretig, *R Statistics Cookbook*, Packt Publishing, 1st Edition, 2019.
2. Prabhanjan N. Tattar, Suresh Ramaiah, B. G. Manjunath, *A Course in Statistics with R*, Wiley, 2018.