ACADEMIC REGULATIONS

COURSE STRUCTURE

AND

DETAILED SYLLABI

For

MASTER OF TECHNOLOGY

In

VLSI

(For the batches admitted from 2019-2020)

CHOICE BASED CREDIT SYSTEM

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)

(Affiliated to JNTU Anantapur, Approved by AICTE
Programs Accredited by NBA; NAAC with 'A' grade)
Sree Sainath Nagar, A.Rangampet, Near Tirupati - 517 102.A.P.

VISION

To be one of the Nation's premier Engineering Colleges by achieving the highest order of excellence in Teaching and Research.

MISSION

- To foster intellectual curiosity, pursuit and dissemination of knowledge.
- To explore students' potential through academic freedom and integrity.
- To promote technical mastery and nurture skilled professionals to face competition in ever increasing complex world.

QUALITY POLICY

Sree Vidyanikethan Engineering College strives to establish a system of Quality Assurance to continuously address, monitor and evaluate the quality of education offered to students, thus promoting effective teaching processes for the benefit of students and making the College a Centre of Excellence for Engineering and Technological studies.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To be a center of excellence in Electronics and Communication Engineering through teaching and research producing high quality engineering professionals with values and ethics to meet local and global demands.

MISSION

- The Department of Electronics and Communication Engineering is established with the cause of creating competent professionals to work in multicultural and multidisciplinary environments.
- Imparting knowledge through contemporary curriculum and striving for development of students with diverse background.
- Inspiring students and faculty members for innovative research through constant interaction with research organizations and industry to meet societal needs.
- Developing skills for enhancing employability of students through comprehensive training process.
- Imbibing ethics and values in students for effective engineering practice.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M. Tech. (VLSI)

PROGRAM EDUCATIONAL OBJECTIVES

After few years of graduation, the graduates of M. Tech. (VLSI) Program would have

PEO1. Enrolled or completed research studies in the core or allied areas of VLSI.

PEO2. Successful entrepreneurial or technical career in the core or allied areas of VLSI.

PEO3. Continued to learn and to adapt to the world of constantly evolving technologies in the core or allied areas of VLSI.

PROGRAM OUTCOMES

On successful completion of the Program, the graduates of M. Tech. (VLSI) will be able to:

PO1. Demonstrate mastery of knowledge in VLSI and other allied areas of the program.

PO2. Design and develop Integrated Circuits/systems/platforms for Digital, Analog and Mixed VLSI applications.

PO3. Select and apply appropriate modern tools, techniques and resources to provide engineering solutions in VLSI and allied areas.

PO4. Independently carry out research to deliver solutions for complex problems in VLSI.

PO5. Communicate effectively in written and oral formats.

PO6. Ability to continuously engage in life-long learning to enhance knowledge and competence.

The Challenge of Change

"Mastery of change is in fact the challenge of moving human attention from an old state to a new state. Leaders can shift attention at the right time and to the right place. The real crisis of our times is the crisis of attention. Those who lead are the ones who can hold your attention and move it in a purposeful way. Transformation is nothing but a shift in attention from one form to another. The form of a beautiful butterfly breaks free from a crawling caterpillar. If you pay enough attention, you would be able to see how the butterfly hides within the caterpillar. The leader points out a butterfly when the follower sees only a caterpillar".

- Debashis Chatterjee

SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
(Affiliated to J.N.T. University Anantapur, Ananthapuramu)

ACADEMIC REGULATIONS
(SVEC-19)

CHOICE BASED CREDIT SYSTEM

M. Tech. Regular Two Year Degree Program
(For the batches admitted from the academic year 2019-2020)

For pursuing Two year degree program of study in Master of Technology (M.Tech) offered by Sree Vidyanikethan Engineering College under Autonomous status and herein after referred to as SVEC:

1. Applicability: All the rules specified herein, approved by the Academic Council, shall be in force and applicable to students admitted from the academic year 2019-2020 onwards. Any reference to "College" in these rules and regulations stands for SVEC.

2. Extent: All the rules and regulations, specified hereinafter shall be read as a whole for the purpose of interpretation and as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. It shall be ratified by Academic Council in the forth coming meeting. As per the requirements of statutory bodies, Principal, SVEC shall be the Chairman, Academic Council.

3. Admission :

3.1. Admission into the Two Year M. Tech. Degree Program:

3.1.1. Eligibility:

A candidate seeking admission into the two year M. Tech Degree Program should have

(i) Passed B.Tech/B.E or equivalent Program recognized by JNTUA, Ananthapuramu, for admission as per the guidelines of Andhra Pradesh State Council of Higher Education (APSCHE).

(ii) A minimum percentage of marks in the qualifying degree as prescribed by the AICTE / UGC or Government at the time of admission.

(iii) Rank/score secured in the PGECET/GATE examination conducted by APSCHE/ MHRD for allotment of a seat by the convener PGECET, for admission.

3.1.2. Admission Procedure:

Admissions are made into the two year M.Tech. Degree Program as per the stipulations of APSCHE, Government of Andhra Pradesh:

(a) By the Convener, PGECET (for Category–A Seats)

(b) By the Management (for Category-B Seats).

4. Programs of study offered leading to the award of M.Tech. Degree and Eligibility:

Following are the two year M.Tech degree Programs of study with specializations, offered by the departments in SVEC leading to the award of M.Tech. degree and the qualifying degree eligible for admission:

Name of the M.Tech specialization	Offered by the Department	Qualifying Degree / Branch eligible for Admission
Electrical Power Systems	EEE	BE/ B.Tech / AMIE in Electrical & Electronics Engineering / Electrical Engineering or equivalent
Power Electronics and Drives		
Digital Electronics and Communication Systems	ECE	BE / B.Tech in ECE / AMIE in ECE, AMIE (Electronics & Telecommunication Engineering) / AMIETE (Electronics & Telematics Engineering)/ Electronics & Computer Engineering/ Electronics/ Electronics & Telematics or equivalent
Communication Systems		
VLSI		BE / B.Tech / AMIE in ECE, / EEE / CSE / Electronics & Computer Engineering / ETE / IT / CSIT / Electronics and Control Engineering / Instrumentation Engineering / Instrumentation Technology / EIE / Electronics Engineering / Bio-Medical Engineering / AMIETE (Electronics & Telematics Engineering)/ Electronics or equivalent
Computer Science	CSE	BE / B.Tech / AMIE in CSE / CSIT / IT / CSSE , M.Sc. (Computer Science), M.Sc. (Information Systems), M. Sc. (Information Technology), MCA or equivalent.
Computer Networks and Information Security		
Software Engineering	IT	

5. Duration of the Program:

5.1 Minimum Duration:

The program will extend over a period of two years leading to award of the Degree of Master of Technology (M.Tech) by JNTUA University, Ananthapuramu. The two academic years are divided into four semesters with two semesters per year. Each semester shall consist of 21 weeks (≥90 working days) having – 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) as suggested by UGC, and Curriculum/Course Structure as suggested by AICTE are followed.

5.2 Maximum Duration:

The student shall complete all the passing requirements of the M.Tech degree program within a maximum duration of 04 years excluding the Gap year. This duration is reckoned from the commencement of the semester into which the student is first admitted to the program.

6. Course Structure:

Each M.Tech Program of study shall comprise of:

- Professional Core courses:

  The list of professional core courses shall be chosen as per the suggestions of the experts, to impart knowledge and skills needed in the concerned specialization of study.

- Professional Elective courses:

  Professional elective courses shall be offered to the students to diversify their spectrum of knowledge and skills. The elective courses can be chosen based on the interest of the student to broaden his individual knowledge and skills.

- Audit Courses: Audit courses shall be offered to the students to diversify their knowledge.

- Projects (Internship, Project work)

7. Credit System: All Courses are to be registered by a student in a Semester to earn Credits. Credits are assigned based on the following norms given in Table 1.

Table 1

Course	Periods/Week	Credits
Theory	01	01
Practical	01	0.5
Internship	--	02
Project Work Phase-I	--	10
Project Work Phase-II	--	16

All Courses are to be registered by a student in a Semester to earn Credits. Credits shall be assigned to each Course in an L: T: P: C (Lecture Hours: Tutorial Hours: Practical Hours: Credits) Structure, based on the following general pattern.

- **Theory Courses:** One Lecture Hour (L) per week in a semester: 01 Credit
- **Practical Courses:** One Practical Hour (P) Per week in a semester: 0.5 Credit
- **Tutorial:** One Tutorial Hour (T) Per week in a semester: 01 Credit
- **Audit Courses:** No **CREDIT** is awarded.
- **Open Elective** (MOOC): 03 Credits

For courses like Internship and Project work, where formal contact periods are not specified, credits are assigned based on the complexity of the work to be carried out. Other student activities like NCC, NSS, Sports, Study Tour, and Guest Lecture etc. shall not carry Credits.

The two year curriculum of any M. Tech Degree Program of study shall have total of **68**credits.

8. Choice Based Credit System (CBCS):

8.1 Choice Based Credit System (CBCS) is introduced in line with UGC guidelines in order to promote:

- Student centered learning
- Students to learn courses of their choice
- Interdisciplinary learning

A Student has a choice of registering for courses comprising program core, Program electives, Open elective through MOOC course.

9. Course Enrollment and Registration

9.1 Each student, on admission shall be assigned to a Faculty Advisor (Mentor) who shall advice and counsel the student about the details of the academic program and the choice of courses considering the student's academic background and career objectives.

9.2 The enrollment of courses in I-Semester will commence on the day of admission. If the student wishes, the student may drop or add courses (vide clause 8) within **three** days before commencement of I-Semester class work and complete the registration process. The student shall enroll for the courses with the help of Faculty Advisor (Mentor). The enrollment of courses in II-Semester will commence 10 days prior to the last instructional day of the I-Semester and complete the registration process for all the remaining theory courses as per program course structure, duly authorized by the Chairman, Board of studies of concerned department.

9.3 If any student fails to register the courses in a semester, he shall undergo the courses as per the program course structure.

9.4 After registering for a course, a student shall attend the classes, satisfy the attendance requirements, earn Continuous Assessment marks and appear for the Semester-end Examinations.

9.5 No elective course shall be offered by a Department unless a minimum of 08 students register for the course.

10. OPEN ELECTIVE (MOOC):

OPEN ELECTIVE (MOOC) is an online course aimed at unlimited participation and open access via the web.

10.1 A Student is offered an Open Elective (MOOC), in the M.Tech II-Semester, and pursued through Massive Open Online Course (MOOC) platforms.

10.2 The student shall confirm registration by enrolling the course within 10 days prior to the last instructional day of the M.Tech I-Semester along with other courses.

10.3 The list of courses along with MOOC service providers shall be identified by the Chairman, BOS, and Head of the Department. The identified Open Elective (MOOC) courses are to be approved by the Chairman, Academic Council.

10.4 The HOD shall appoint one faculty member as **mentor** during the M.Tech I-Semester for each Open Elective Course registered through MOOC.

10.5 There shall be ONLY semester-end examination for open elective (MOOC) course. It shall be evaluated by the department through ONLINE with 50 multiple choice questions for 100 marks. The department shall prepare the Question Bank for Conducting the ONLINE Open Elective (MOOC) Examination.

11. Break of Study from a Program (Gap Year)

11.1 A student is permitted to go on break of study for a maximum period of one year.

11.2 The student shall apply for break of study in advance, in any case, not later than the last date of the first assessment period in a semester. The gap year concept is introduced for start-up (or) incubation of an idea, National/International Internships, professional Volunteering and chronic illness. The application downloaded from the website and duly filled in by the student shall be submitted to the Principal through the Head of the department. A committee shall be appointed by the Principal in this regard. Based on the recommendations of the committee, Principal shall decide whether to permit the student to avail the gap year or not.

11.3 The students permitted to rejoin the program after break of study shall be governed by the Curriculum and Regulations in force at the time of rejoining.

The students rejoining in new regulations shall apply to the Principal in the prescribed format through Head of the Department, at the beginning of the readmitted semester for registering additional/equivalent courses to comply with the curriculum in-force.

11.4 The one year period of break of study shall not be counted for the maximum period for the award of the degree (i.e 05 years shall be the maximum period for the award of degree for the students availing Gap Year).

11.5 If a student has not reported to the college after completion of approved period of break of study without prior intimation, he is deemed to be detained in that semester. Such students are eligible for readmission into the semester when offered next.

12. Examination System: All components in any Program of study shall be evaluated through internal evaluation and/or an external evaluation conducted as semester-end examination.

12.1. Distribution of Marks:

Sl. No.	Course	Marks	Examination and Evaluation	Scheme of examination
1.	Theory	60	Semester-end examination of 3 hours duration (External evaluation)	The examination question paper in theory courses shall be for a maximum of 60 marks. The question paper shall be of descriptive type with 10 questions each of 12 marks, taken two from each unit. Each unit will have internal choice and 5 questions shall be answered, one from each unit.
		40	Mid-term Examination of 2 hours duration (Internal evaluation).	Two mid-term examinations each for 40 marks are to be conducted. For a total of 40 marks, 80% of better one of the two and 20% of the other one are added and finalized. **Mid-I:** After first spell of instruction (I & II Units). **Mid-II**: After second spell of instruction (III, IV & V Units). The question paper shall be of descriptive type with 5 essay type questions each of 10 marks, out of which 3 are to be answered and evaluated for 30 marks. There shall be also 5 short answer questions each of 2 marks, all are to be answered and evaluated for 10 marks.

Sl. No.	Course	Marks	Examination and Evaluation		Scheme of examination
2	Laboratory	50	Semester-end Lab Examination for 3 hours duration (External evaluation)		The examination will be conducted by the faculty member handling the laboratory (Examiner-2) and another faculty member (Examiner-1) appointed by the Chief Controller of examinations.
		50	30	Day-to-Day evaluation for Performance in laboratory experiments and Record. (Internal evaluation).	Two laboratory examinations, which include Day-to-Day evaluation and Practical test, each for 50 marks are to be evaluated by the faculty members handling the laboratory. For a total of 50 marks 80% of better one of the two and 20% of the other one are added and finalized. **Laboratory examination-I:** Shall be conducted just before FIRST mid-term examinations. **Laboratory examination-II:** Shall be conducted just before SECOND mid-term examinations.
			20	Practical test (Internal evaluation).	
3	Audit Courses	--	--		As detailed in 12.2.1
4	Internship	100	Semester-end Examination		100 marks are allotted for Internship During semester-end evaluation by the Department Evaluation Committee (**DEC**) as given in 12.2.2.
5	Open Elective (MOOC)	100	Semester-end Examination		The evaluation shall be done by the department through ONLINE with 50 multiple choice questions.
6	Project Work Phase-I	100	50	Internal evaluation	Continuous evaluation shall be done by the Project Evaluation Committee (**PEC)** as given in 12.2.3.1
			50	Semester-end evaluation	Project Work Viva-Voce Examination shall be conducted by a Committee at the end of the semester as given in 12.2.3.1
7	Project Work Phase-II	300	150	Internal evaluation	Continuous evaluation shall be done by the Project Evaluation Committee (**PEC)** as given in 12.2.3.2
			150	Semester-end evaluation	Project Work Viva-Voce Examination shall be conducted by a Committee at the end of the semester as given in 12.2.3.2

12.2 Audit Course/ Internship and Project Work Evaluation:

12.2.1. Audit Course:

Audit courses carry "ZERO" credits. There shall be **NO Internal Examination** and **Semester-end examination**. However, ATTENDANCE in Audit courses shall be considered while calculating aggregate attendance in a semester. The student should study all the audit courses, and it will be indicated in the GRADE Sheet.

12.2.2. Internship:

The student shall undergo **Internship** in an Industry/National Laboratories/Academic Institutions relevant to the respective branch of study. This course is to be registered during II-Semester and taken up during the summer vacation after completion of the II-Semester, for a period of FOUR weeks duration. The Industry training/Internship shall be submitted in a Report form, and a presentation of the same shall be made

before a Department Evaluation Committee (DEC) and it should be evaluated for 100 marks. The DEC shall consist of the Head of the Department, the concerned Supervisor and a Senior Faculty Member of the Department. The DEC is constituted by the Chief Controller of Examinations on the recommendations of the Head of the Department. There shall be NO internal marks for Internship. The Internship shall be evaluated at the end of the III-Semester.

12.2.3. Project Work:

12.2.3.1. The Project Evaluation Committee (PEC) consisting of concerned supervisor and two senior faculty members shall monitor the progress of the project work of the student. The PEC is constituted by the Principal on the recommendations of the Head of the Department. Project Work Phase–I is to be completed in the III-Semester. A Student has to identify the topic of the Project Work, collect relevant Literature, preliminary data, implementation tools/ methodologies etc., and perform a critical study and analysis of the problem identified and submit a Report.

(i) **Internal Evaluation:** The Internal Evaluation of Project work Phase-I shall be made by the PEC on the basis of TWO project reviews on the topic of the project. Each review shall be conducted for a maximum of "50" marks. For a total of 50 marks, 80% of better one of the two and 20% of the other one are added and finalized.

(ii) **Semester-end Evaluation:** The semester-end Project Work Phase-I Viva-Voce examination shall be conducted by the concerned guide and a senior faculty member recommended by the Head of the Department and appointed by the Chief Controller of Examinations.

12.2.3.2 A student shall continue to undertake the Project Work Phase–II during theIV Semester by undertaking practical investigations, implementation, analysis of results, validation and report writing. The student shall submit a Project report at the end of the semester after approval of the PEC.

(i) **Internal Evaluation:** The Internal Evaluation of Project work Phase-II shall be made by the PEC by conducting TWO project reviews on the progress, presentations and quality of work. Each review shall be conducted for a maximum of "150" marks. For a total of 150 marks, 80% of better one of the two and 20% of the other one are added and finalized.

(ii)**Semester-end Evaluation:** A candidate shall be allowed to submit the dissertation on the recommendations of the PEC. Three copies of the dissertation certified in the prescribed format by the concerned Supervisor and HOD shall be submitted to the Department. One copy is to be submitted to the Chief Controller of Examinations and one copy to be sent to the examiner. The examiner shall be nominated by the Chief Controller of the Examinations from the panel of THREE examiners submitted by the Department for a maximum of 05 students at a time for adjudication.

If the report of the examiner is favorable, Semester-end Project Work Phase-II Viva-Voce Examination shall be conducted by a Committee consisting of External examiner (nominated by the Chief Controller of Examinations), HOD and concerned Supervisor at the end of the IV Semester.

If the report of the examiner is not favorable, the dissertation should be revised and resubmitted after a minimum period of three months.

12.2.3.3 The students who fail in Project work Phase-I (or) Phase-II Viva-Voce examination shall have to re-appear for the Viva-Voce examination after three months. Extension of time for completing the project is to be obtained from the Chairman, Academic Council, SVEC (Autonomous).

12.2.3.4 Change of the project work topic shall be permitted only in Project Work Phase-I, within FOUR weeks after commencement of the III-Semester with the approval of the PEC.

12.3. Eligibility to appear for the semester-end examination:

12.3.1 A student shall be eligible to appear for semester-end examinations if he acquires a minimum of 75% of attendance in aggregate of all the courses in a semester.

12.3.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

12.3.3 Shortage of attendance below 65% in aggregate shall in no case be condoned.

12.3.4 Students whose shortage of attendance is not condoned in any semester shall not be eligible to take their semester-end examination and their registration shall stand cancelled.

12.3.5 A student shall not be promoted to the next semester unless he satisfies the attendance requirements of the semester, as applicable. The student may seek readmission for the semester when offered next. He will not be allowed to register for the courses of the semester while he is in detention.

12.3.6 A stipulated fee shall be payable to the college towards condonation of shortage of attendance.

12.4. Evaluation:

Following procedure governs the evaluation.

12.4.1. Marks for components evaluated internally by the faculty should be submitted to the Controller of Examinations one week before the commencement of the semester-end examinations. The marks for the internal evaluation components shall be added to the external evaluation marks secured in the semester-end examinations, to arrive at total marks for any course in that semester.

12.4.2. Performance in all the courses is tabulated course-wise and shall be scrutinized by the Results Committee and moderation is applied if needed and course-wise marks are finalized. Total marks obtained in each course are converted into letter grades.

12.4.3. Student-wise tabulation shall be done and individual grade sheet shall be generated and issued.

12.5. Personal verification / Revaluation / Recounting:

Students shall be permitted for personal verification/request for recounting/ revaluation of the semester-end examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records shall be updated with changes if any and the student shall be issued a revised grade sheet. If there are no changes, the student shall be intimated the same through a notice.

12.6. Supplementary Examination:

In addition to the regular semester-end examinations conducted, the College may also schedule and conduct supplementary examinations for all the courses of other semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

13. Re-Registration for Improvement of Internal Marks:

Following are the conditions to avail the benefit for improvement of internal evaluation marks.

13.1 The student should have completed all the course work and obtained examinations results for I, II and III semesters.

13.2 If the student has **failed** in the examination due to internal evaluation marks secured being less than 50%, he shall be given one chance for a maximum of 3 theory courses for improvement of internal evaluation marks.

13.3 The candidate has to register for the chosen courses and fulfill the academic requirements.

13.4 For each course, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D/ Challan in favour of the Principal, Sree Vidyanikethan Engineering College payable at Tirupati along with the requisition through the concerned Head of the Department.

13.5 If a student avails the benefit for Improvement of Internal evaluation marks, the internal evaluation marks as well as the semester-end examinations marks secured in the previous attempt(s) for the re-registered courses stands cancelled.

14. Academic Requirements for Completion of M.Tech degree Program:

The following academic requirements have to be satisfied in addition to the attendance requirements for completion of M.Tech degree Program.

14.1 A student shall be deemed to have satisfied the minimum academic requirements for each theory, laboratory and project work, if he secures not less than 40% of marks in the semester-end examination and a minimum of 50% of marks in the sum total of the internal evaluation and semester-end examination taken together. For the ***internship*** and ***open elective (MOOC) courses***, he should secure not less than 50% of marks in the semester-end examination.

14.2 A student shall register for all the 68credits and earn all the 68 credits. Marks obtained in the 68credits shall be considered for the calculation of the DIVISION based on CGPA.

14.3 A student who fails to earn 68credits as indicated in the curriculum within **four** academic years from the year of his admission shall forfeit his seat in M.Tech. Program and his admission stands cancelled.

15. Transitory Regulations:

Students who got detained for want of attendance (**or**) who have not fulfilled academic requirements (**or**) who have failed after having undergone the Program in earlier regulations (**or**) who have discontinued and wish to continue the Program are eligible for admission into the unfinished semester from the date of commencement of class work with the same (**or**) equivalent courses as and when courses are offered and they will be in the academic regulations into which they are presently readmitted.

A regular student has to satisfy all the eligibility requirements within the maximum stipulated period of **four years** for the award of M.Tech Degree.

16. Grades, Grade Point Average and Cumulative Grade Point Average:

16.1. Grade System: After all the components and sub-components of any course (including laboratory courses) are evaluated, the final total marks obtained shall be converted to letter grades on a "**10 point scale**" as described below.

Grades conversion and Grade points allotted

% of Marks obtained	Grade	Description of Grade	Grade Points (GP)
≥ 95	O	Outstanding	10
≥ 85 to < 95	S	Superior	9
≥ 75 to < 85	A	Excellent	8
≥ 65 to < 75	B	Very Good	7
≥ 55 to < 65	C	Good	6
≥ 50 to <55	D	Pass	5
< 50	F	Fail	0
Not Appeared	N	Absent	0

Pass Marks:

A student shall be declared to have passed theory course, laboratory course and project work if he secures minimum of 40% marks in Semester-end examination, and a minimum of 50% marks in the sum total of internal evaluation and Semester-end examination taken together. For the seminar, he shall be declared to have passed if he secures minimum of 50% of marks in the semester-end examinations. Otherwise he shall be awarded fail grade - **F** in such a course irrespective of internal marks. **F** is considered as a fail grade indicating that the student has to pass the semester-end examination in that course in future and obtain a grade other than **F** and **N** for passing the course.

16.2 Semester Grade Point Average (SGPA): SGPA shall be calculated as given below on a "10 point scale" as an index of the student's performance:

$$SGPA = \frac{\sum(C\ X\ GP)}{\sum C}$$

Where "C" denotes the "credits" assigned to the courses undertaken in that semester and "GP" denotes the "grade points" earned by the student in the respective courses.

Note: SGPA is calculated only for the candidates who appeared in the semester-end regular examinations in a particular semester:

16.3. Cumulative Grade Point Average (CGPA):

The CGPA shall be calculated for a candidate appeared in the Semester-end examinations for all the courses (including Regular & Supplementary) till that semester. The CGPA will be displayed in the Grade sheet of the Regular Semester-end examinations and also in the consolidated Grade Sheet issued at the end of the program. The CGPA is computed on a 10 point scale as given below:

$$CGPA = \frac{\sum(C\ X\ GP)}{\sum C}$$

where C denotes the credits assigned to courses undertaken up to the end of the Program and GP denotes the grade points earned by the student in the respective courses.

17. Grade Sheet: A grade sheet (Marks Memorandum) shall be issued to each student on his performance in all courses registered in that semester indicating the **SGPA and CGPA.**

18. Consolidated Grade Sheet: After successful completion of the entire Program of study, a Consolidated Grade Sheet indicating performance of all academic years shall be issued as a final record. Duplicate Consolidated Grade Sheet will also be issued, if required, after payment of requisite fee.

19. Award of Degree: The Degree shall be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Ananthapuramu on the recommendations of the Chairman, Academic Council, SVEC (Autonomous).

19.1. Eligibility: A student shall be eligible for the award of M.Tech Degree if he fulfills all the following conditions:

- Registered and successfully completed all the components prescribed in the Program of study to which he is admitted.
- Successfully acquired the minimum required credits as specified in the curriculum corresponding to the Program of study within the stipulated time.
- Obtained CGPA greater than or equal to 5.0 (Minimum requirement for declaring as passed).
- Has NO DUES to the College, Hostel, Library etc. and to any other amenities provided by the College.
- No disciplinary action is pending against him.

19.2. Award of Division: Declaration of division is based on CGPA.

Awarding of Division

CGPA	Division
> = 7.0	First Class with Distinction
> = 6.0 and < 7.0	First Class
> = 5.0 and < 6.0	Second Class

20. Additional Academic Regulations:

20.1 A student may appear for any number of supplementary examinations within the stipulated time to fulfill regulatory requirements for award of the degree.

20.2 In case of malpractice/improper conduct during the examinations, guidelines shall be followed as shown in the **ANNEXURE-I**.

20.3 When a student is absent for any examination (Mid-term or Semester-end) he shall be awarded **zero** marks in that component (course) and grading will be done accordingly.

20.4 When a component is cancelled as a penalty, he shall be awarded zero marks in that component.

21. Withholding of Results:

If the candidate has not paid dues to the College/University (or) if any case of indiscipline is pending against him, the result of the candidate shall be withheld and he will not be allowed/promoted to the next higher semester

22. Amendments to regulations:

The Academic Council of SVEC (Autonomous) reserves the right to revise, amend, or change the Regulations, Scheme of Examinations, and / or Syllabi or any other policy relevant to the needs of the society or industrial requirements etc., with the recommendations of the concerned Board(s) of Studies.

23. General:

The words such as "he", "him", "his" and "himself" shall be understood to include all students irrespective of gender connotation.

Note: *Failure to read and understand the regulations is not an excuse.*

ANNEXURE-I

GUIDELINES FOR DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

Rule No.	Nature of Malpractices/ Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the course of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester. The Hall Ticket of the candidate is to be cancelled.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including labs and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester. The candidate is also debarred for four consecutive semesters from class work and all Semester-end examinations, if his involvement is established. Otherwise, The candidate is debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course only.

6.	Refuses to obey the orders of the Chief Controller of Examinations/Controller of Examinations/any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the Controller of Examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Controller of Examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester. If the candidate physically assaults the invigilator/Controller of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred and forfeits the seat.

Note: Whenever the performance of a student is cancelled in any course(s) due to Malpractice, he has to register for Semester-end Examinations in that course(s) consequently and has to fulfill all the norms required for the award of Degree.

Course Structure for M. Tech. (VLSI)
SVEC-19

I-Semester

Sl. No.	Course Code	Course Title	Contact Periods per week				C	Scheme of Examinations Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1.	19MT15701	Analog CMOS VLSI Design	3	-	-	3	3	40	60	100
2.	19MT15702	Device Modeling	3	-	-	3	3	40	60	100
3.	19MT15703	Digital CMOS VLSI Design	3	-	-	3	3	40	60	100
Program Elective-1			3	-	-	3	3	40	60	100
4.	19MT15704	Computational Methods in Microelectronics								
	19MT15705	IC Fabrication								
	19MT15706	VLSI Design Verification and Testing								
Program Elective-2			3	-	-	3	3	40	60	100
5.	19MT15707	FPGA Architectures								
	19MT15708	Low Power CMOS VLSI Design								
	19MT15709	Mixed Signal Design								
6.	19MT10708	Research Methodology and IPR	2	-	-	2	2	40	60	100
7.	19MT15731	Analog CMOS VLSI Design Lab	-	-	4	4	2	50	50	100
8.	19MT15732	Digital CMOS VLSI Design Lab	-	-	4	4	2	50	50	100
Total			**17**	**-**	**8**	**25**	**21**	**340**	**460**	**800**
9.	19MT1AC01	Technical Report Writing	2	-	-	2	-	-	-	-

II-Semester

Sl. No.	Course Code	Course Title	Contact Periods per week				C	Scheme of Examinations Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1.	19MT25701	Nano Materials and Nanotechnology	3	-	-	3	3	40	60	100
2.	19MT25702	Physical Design Automation	3	-	-	3	3	40	60	100
Program Elective-3			3	-	-	3	3	40	60	100
3.	19MT25703	Co Design								
	19MT25704	Memory Technologies								
	19MT25705	System-on-Chip Design								
Program Elective-4			3	-	-	3	3	40	60	100
4.	19MT25706	Communication Buses and Interfaces								
	19MT25707	Network-on-Chip Design								
	19MT25708	RF IC Design								
5.	19MT2MOOC	Open Elective (MOOC)	-	-	-	-	3	-	100	100
6.	19MT25731	Physical Design Automation Lab	-	-	4	4	2	50	50	100
7.	19MT25732	Nano Materials and Nanotechnology Lab	-	-	4	4	2	50	50	100
Total			**12**	**-**	**8**	**20**	**19**	**260**	**440**	**700**
8.	19MT2AC01	Statistics with R	2	-	-	2	-	-	-	-

III-Semester

Sl. No.	Course Code	Course Title	Contact Periods per week				C	Scheme of Examinations Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1.	19MT35731	Internship	-	-	-	-	2	-	100	100
2.	19MT35732	Project Work Phase-I	-	-	20	20	10	50	50	100
Total			**-**	**-**	**20**	**20**	**12**	**50**	**150**	**200**

IV-Semester

Sl. No.	Course Code	Course Title	Contact Periods per week				C	Scheme of Examinations Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1.	19MT45731	Project Work Phase-II	-	-	32	32	16	150	150	300
Total			**-**	**-**	**32**	**32**	**16**	**150**	**150**	**300**
Total Credits							**68**	**-**	**--**	**--**
Grand Total Marks:										**2000**

M. Tech. – I Semester
(19MT15701) ANALOG CMOS VLSI DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Semiconductor Devices and Circuits and VLSI design at UG Level.

COURSE DESCRIPTION:

MOS Device physics; Characteristics of amplifiers; Feedback circuits and operational amplifiers; Stability and frequency compensation of operational amplifiers; Nonlinear Analog circuits & other applications

COURSE OBJECTIVES:

CEO1: To provide advanced knowledge in Analog VLSI circuits.
CEO2: To impart analysis, problem solving, design and application skills in Analog IC Design.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:

CO1. Design Single Stage amplifiers, differential amplifiers, develop noise models of MOSFETs for high speed designs.
CO2. Design and Develop Feedback Amplifiers and Operational Amplifiers for linear circuits.
CO3. Apply stability and frequency compensation techniques to multistage systems and design band gap references.
CO4. Understand various Design Aspects of switched capacitor circuits, oscillators and PLL.

DETAILED SYLLABUS:

Unit-I: Basic MOS Device Physics and Single Stage Amplifiers (Hours: 11)
Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second-Order Effects.
Single Stage Amplifiers: Basic Concepts, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential Amplifiers-Single Ended and Differential Operation, Basic Differential Pair, Passive and Active Current Mirrors.

Unit-II: Frequency Response and Noise Characteristics of Amplifiers (Hours: 08)
Frequency Response-General Considerations, Common-Source Stage, Source follower, Common Gate Stage, Cascode Stage, Differential pair.
Noise-Statistical Characteristics of Noise, Noise in Single Stage Amplifiers, Noise in Differential Pairs.

Unit-III: Feedback Circuits and Operational Amplifiers (Hours: 10)
Feedback Circuits - General considerations, Feedback Topologies, Effect of Loading, Effect of Feedback on Noise.
Operational Amplifiers - General considerations, One-stage Op Amps, Two - stage Op Amps, Gain Boosting, Input range limitations, slew rate, power supply rejection, Noise in Op Amps.

Unit-IV: Stability & Frequency Compensation and Bandgap References
(Hours: 08)

Stability & Frequency Compensation: General considerations, Multipole Systems, Phase Margin, Frequency Compensation, Compensation of Two-Stage Op Amps.
Bandgap References: Supply-Independent Biasing, Temperature-independent References, PTAT Current Generation, Constant - Gm Biasing, Speed and Noise Issues.

Unit-V: Nonlinear Analog circuits & other applications (Hours: 08)
Sampling Switches, Switched-Capacitor Amplifiers, Switched capacitor integrator, Ring oscillators, Simple PLL.

Total Hours: 45

TEXT BOOK:

1. Behzad Razavi, "*Design of Analog CMOS Integrated Circuit*", Tata-Mc Graw Hill, 14th Reprint 2008.

REFERENCE BOOKS:

1. D.A. John & Ken Martin, *"Analog Integrated Circuit Design",* John Wiley, 1997.
2. Philip Allen & Douglas Holberg, *"CMOS Analog Circuit Design",* Oxford University Press, 2002.

M. Tech. - I Semester
(19MT15702) DEVICE MODELING

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Semiconductor Devices and Circuits at UG Level

COURSE DESCRIPTION:

MOS Transistor; Small Dimension Effects; Ion Implanted Channels; MOS Transistor in Static and Dynamic operations and its Small signal Modeling.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in various MOS Structures.
CEO2: To develop skills in design, analysis and problem solving related to regions of inversion and development of high performance MOS transistors.
CEO3: Apply knowledge and skills for performance analysis in the design of MOS Structures with respect to small dimension effects.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze the multi terminal MOS device, MOS transistor to improve performance characteristics of digital IC's.
CO2. Analyze small dimensional effects in MOS with Ion implanted Channels for VLSI systems.
CO3. Develop Quasi static Model and Non Quasi static Models for low, medium and high frequencies.

DETAILED SYLLABUS:

UNIT-I **(Hours: 10)**

Basic Device Physics-I:
Two Terminal MOS Structure: Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Small signal capacitance; C-V Characteristics.
Three Terminal MOS Structure: Contacting the inversion layer, Body effect, Regions of inversion, Pinch-off voltage.

UNIT-II **(Hours: 12)**

Basic Device Physics-II:
Four Terminal MOS Transistor: Transistor regions of operation, general charge sheet models, regions of inversion in terms of terminal voltage, strong inversion, weak inversion, moderate inversion, interpolation models, effective mobility, temperature effects, breakdown p-channel MOS FET, enhancement and depletion type, model parameter values, model accuracy .

UNIT-III **(Hours: 10)**

MOS Transistor with Ion-Implanted Channels: Enhancement of nMOS, Depletion nMOS, Enhancement pMOS.
Small dimension effects: Channel length modulation, barrier lowering, two dimensional charge sharing and threshold voltage, punch-through, carrier velocity saturation, hot carrier effects, scaling, effects of surface and drain series resistance, effects due to thin oxides and high doping. Sub threshold regions, Short channel effects.

UNIT-IV **(Hours: 07)**

MOS Transistor in Dynamic Operation: Large Signal modeling: Quasi static operation, Terminal currents in Quasi static operation, Evaluation of Charges in Quasi static operation, Transit time under DC conditions, Limitations of Quasi static Model, Non Quasi static Analysis.

UNIT-V **(Hours: 06)**

Small Signal Modeling for Low, Medium And High Frequencies: low, Medium frequency small signal model for the intrinsic part, Small signal model for Extrinsic Part, A complete Quasi static Model, Y-Parameter models, Non Quasi static Models.

Total Hours: 45

TEXT BOOK:

1. Y. Tsividis, *"Operations and Modeling of the MOS Transistor",* Oxford university Press, 3rd edition, 2012.

REFERENCE BOOKS:

1. Trond Ytterdal, Yuhua Cheng and Tor Fjeldly *"Device Modeling for Analog and RF CMOS Circuit Design"* Wiley Publication, 2003.
2. Donald A Neamen and Dhrubes Biswas *"Semiconductor Physics and Devices"* Special Indian Edition, 4th edition, 2012.

M. Tech. I - Semester
(19MT15703) DIGITAL CMOS VLSI DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Digital IC Applications and VLSI Design at UG Level.

COURSE DESCRIPTION:

Introduction to MOS transistors; Characteristics of CMOS digital circuits; Transistor sizing; memory design; Design strategies; Design of subsystems.

COURSEOBJECTIVES:

CEO1: To impart in-depth knowledge in MOS transistor Integrated Circuits.
CEO2: To develop skills in design and development, analysis, problem solving and research in Digital Systems.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze the characteristics of CMOS Inverter and Design combinational and sequential logic circuits using various design styles.
CO2. Analyze timing issues to improve the performance of sequential logic circuits.
CO3. Design memories and sub systems using CMOS logic for high speed networks.
CO4. Understand design methodologies and tools at various levels of abstraction.

DETAILED SYLLABUS:

Unit – I: CMOS Inverter Characteristics and Design Styles (Hours: 09)
MOS Inverters: Introduction, Definitions and Properties, Static CMOS Inverter, Static and Dynamic Power Dissipation, CMOS inverter delay time definitions and calculations
Designing Combinational Logic Gates in CMOS: Introduction, Static CMOS Design, Dynamic CMOS Design, Domino and NORA logic, Power Consumption in CMOS Gates.

Unit – II: Designing Sequential Logic Gates in CMOS (Hours: 10)
Introduction, Static Sequential Circuits, Dynamic Sequential Circuits, Non-Bistable Sequential Circuit, Logic Style for Pipelined Structures.
Timing Issues in Digital Circuits: Introduction, Clock Skew and Sequential Circuit Performance, Clock Generation and Synchronization.

Unit - III: High Speed Network and Memory Design (Hours: 09)
Methods of Logical Effort for transistor sizing - Power consumption in CMOS Gates, Low power CMOS design. CMOS Memory design – SRAM, DRAM.

Unit – IV: Subsystem Design Process (Hours: 09)
General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Multipliers, modified Booth's algorithm.

Unit - V: Design Methodology and Tools (Hours: 08)
Introduction, Structured Design Strategies, Design Methods, Design Flows, Design Economics, Data Sheets and Documentation.

Total Hours: 45

TEXT BOOKS:

1. Jan M Rabaey, "*Digital Integrated Circuits*", 2nd Edition, Pearson Education, 2003.
2. Sung-Mo Kang & Yusuf Leblebici, "*CMOS Digital Integrated Circuits*" McGraw Hill, 3rd edition, 2003.
3. Kamran Eshranghian, Douglas A.Pucknell and Sholeh Eshranghian", *Essential of VLSI Circuits and Systems"*, PHI, 1st edition, 2005.
4. Neil H. E. Weste, David Money Harris, *"CMOS VLSI Design-A Circuit and Systems Perspective",* Pearson 4th Edition,2011.

REFERENCE BOOKS:

1. Eugene D Fabricus, *"Introduction to VLSI Design*," McGraw Hill International Edition, 1990.
2. John P.Uyemura*, "Introduction to VLSI Circuits and Systems",* Wiley Edition, 2002.

M. Tech. – I Semester
(19MT15704) COMPUTATIONAL METHODS IN MICROELECTRONICS
(Program Elective -1)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Mathematics at UG Level.

COURSE DESCRIPTION:

Linear and Nonlinear Systems modeling; Approximation; Interpolation; Curve Fitting; Numerical Integration; Finite Difference Techniques; Initial Value problems; Energy Methods and Minimization; Finite Element Methods; Dynamic methods; Method of Characteristics; Finite Volume Methods; Grid Generation and Error Estimation; Device and Process Simulation; Layout and Yield estimation algorithms; Symbolic analysis and Synthesis of Analog ICs.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in Computational Methods for CAD Tools Design.
CEO2: To develop skills in design, analysis and problem solving in high performance Tools Design.
CEO3: To apply knowledge and skills of Computational Methods for development of New Microelectronics CAD Tools.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Apply basic computational tools applied to Finite Difference Techniques, Initial Value Problems, Finite Element Methods to evaluate accurate performance parameters.
CO2. Classify the partial differential equations and use the Method of Characteristics and finite volume methods to perform investigations in engineering.
CO3. Apply Grid generation and refinement algorithms to reduce the error in estimation while evaluating the structures by using solutions of initial and final value problems in computational tools.
CO4. Analyze and apply device and process simulation to perform synthesis of Analog ICs at various levels of abstraction for improving yield.

DETAILED SYLLABUS:

Unit I – Basic Computation Tools (Hours: 12)
Linear Systems and Matrices – Matrix Formalities, Condition of Matrix Systems, Techniques for Matrix Solution, Mixed Boundary Condition. Non linear Systems – Scalar Equations, Matrix Equations. Approximation, Interpolation, Curve Fitting, Numerical Integration.

Unit II – Computational Tools for Applications (Hours: 07)
Finite Difference Techniques, Initial Value Problems, Finite Element Methods.

Unit III – Advanced Computational Tools (Hours: 07)
Method of Characteristics – Classification of Partial Differential Equations, Investigations in Engineering, Finite volume Methods – Direct Analysis.

Unit IV – Grid Generation and Error Estimates (Hours: 10)
Grid generation, Triangulation, errors and mesh Selection, Refinement Algorithms, Mesh Redistribution, Moving Grids.

Unit V – Applications to Device and Process Simulation (Hours: 09)
Applications to device and process simulation, Layout algorithms, Yield estimation algorithms, Symbolic analysis and Synthesis of Analog ICs.

Total Hours: 45

TEXT BOOKS:

1. Herbert Koenig, *"Modern Computational methods",* CRC Press, 1988.
2. Graham F. Carey, *"Computational Grids: generations, adaptation & Solution Strategies",* CRC Press, 1997.
3. L.Pallage, R.Rohrer and C.Visweswaraiah, *"Electronic Circuit and System Simulation Methods"*, McGraw Hill, 1995.

REFERENCE BOOK:

1. Naveed A. Sherwani, *"Algorithms for VLSI Physical Design Automation",* Kluwer Academic Publishers, 1993.

ADDITIONAL LEARNING RESOURCES

https://www.coursebuffet.com/course/805/nptel/computational-techniques-iit-madras
https://nptel.ac.in/downloads/103106074/

M. Tech. – I Semester
(19MT15705) IC FABRICATION
(Program Elective – 1)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Engineering Physics, Chemistry, Material Science, VLSI Design at UG Level

COURSE DESCRIPTION:

Crystal Growth, Wafer Preparation, Epitaxy and Oxidation, Lithography and Reactive Plasma Etching, Deposition, Diffusion, Ion Implantation, Metallization, Analytical, Assembly and Packaging Techniques.

COURSE OBJECTIVES:

CEO1: To provide advanced knowledge in IC Fabrication Processes.
CEO2: To impart analytical skills on Wafer preparation, Lithography, Etching, Diffusion and Packaging.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze Wafer preparation methods, oxidation Techniques, Lithography, Etching techniques Deposition, Diffusion and Ion-Implantation for accurate integrated chip fabrication.
CO2. Select and Apply appropriate metallization choices to compensate problems in electrical interconnectivity in multi metal layer process Fabrication.
CO3. Apply various assembling and packaging techniques for obtaining the required functionality at higher level abstraction.

DETAILED SYLLABUS:

Unit - I: Crystal Growth, Wafer Preparation, Epitaxy and Oxidation **(Hours: 10)**

Clean room and safety requirements, Electronic grade silicon – Czochralski crystal growing – silicon shaping – Vapour phase Epitaxy – Molecular beam epitaxy - Epitaxial Evaluation – Growth mechanism and kinetics – Thin oxides – Oxidation Techniques and systems – Oxide properties – Redistribution of dopants at interface – Oxidation of polysilicon – Oxidation induced effects.

Unit - II: Lithography and Reactive Plasma Etching **(Hours: 10)**

Mask Making – Optical lithography – Electron lithography – X-ray lithography – Ion lithography – Plasma properties– Feature size control and Anisotropic Etch mechanism – Properties of Etch Processes – Reactive plasma etching Techniques and Equipments - Specific Etch Processes.

Unit - III: Deposition, Diffusion, Ion Implantation **(Hours: 09)**

Deposition process – polysilicon - Plasma Assisted deposition – models of diffusion in solids – Fick's one dimensional diffusion equation – Atomic diffusion mechanism – measurement techniques – Range theory – Implantation equipment – Annealing – Shallow junctions – High Energy Implantation.

Unit - IV: Metallization **(Hours: 08)**

Metallization applications – Metallization choices –Physical Vapor Deposition– Patterning – Metallization problems – New role of metallization – Metallization systems – sputtering – problems associated with Al – Cu interconnect – Comparison of RC delay of Polysilicon.

Unit - V: Analytical, Assembly and Packaging Techniques of VLSI Devices **(Hours: 08)**

Analytical beams – Beams specimen interaction – Chemical methods – package types – packing design considerations – VLSI assembly technology – Package Fabrication Technology.

Total Hours: 45

TEXT BOOKS:

1. S.M.Sze "*VLSI Technology*", Tata Mcgraw Hill, 2nd edition, 1988.
2. Sorab. K. Gandhi "*VLSI Fabrication and Principles*", John wiley and sons, 1983.

REFERENCES BOOKS :

1. Amar Mukherjee "*Introduction to NMOS & CMOS VLSI system Design*", Prentice Hall, 1986.
2. Mccanny and J.C.White "*VLSI Technology and design*", Academic Press, 1987.
3. Dasgupta "*VLSI Technology*", Pearson Education Pvt Ltd 2001.

ADDITIONAL LEARNING RESOURCES

1. https://nptel.ac.in/courses/108108111/3
2. https://b-ok.cc/book/1081033/18f7df

M. Tech. - I/II Semester
(19MT15706) VLSI DESIGN VERIFICATION AND TESTING
(Program Elecive-1)
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Courses on VLSI Design, Digital IC Applications at UG Level.

COURSE OBJECTIVES:

CEO1: To impart in-depth knowledge in generation of test vectors for digital systems.
CEO2: To analyze and test the various faults in digital system design and develop fault free applications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze Modeling of Digital Circuits at various levels of abstraction and various types of logic Simulations.
CO2. Understand the various fault models, reduction techniques to apply for fault sampling and simulation.
CO3. Apply the automatic test generation techniques for testing Single Stuck at Faults and bridging faults in digital circuits.
CO4. Analyze the various testing approaches and Built-In Self Test architectures for testing digital circuits.

DETAILED SYLLABUS:

Unit –I: Introduction to Testing (Hours: 08)
Modeling-Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

Unit–II: Fault Modeling and Simulation (Hours: 09)
Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, Fault Simulation Techniques, Fault Sampling.

Unit-III: Testing for Stuck Faults (Hours: 09)
ATG for SSFs in Combinational Circuits and Sequential Circuits, Detection of Non feedback and Feedback Bridging Faults.

Unit–IV: Design for Testability (Hours: 09)
Controllability and Observability, Scan-Based Designs and Architecture, Board-Level and System-Level DFT Approaches, Compression Techniques, Syndrome Testing and Signature Analysis.

Unit-V: Built-In Self Test (Hours: 10)
Introduction to BIST Concepts, Test - Pattern Generation, off-line BIST Architectures, Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO.

Total Hours: 45

TEXT BOOK:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, *"Digital Systems Testing and Testable Design",* Wiley, 1st Edition, 1994.

REFERENCE BOOKS:

1. Alfred L. Crouch, *"Design for Test for Digital ICs & Embedded Core Systems",* Prentice Hall PTR, 1st Reprint Edition, 1999.
2. Robert J.Feugate, Jr., Steven M.Mclntyre, "*Introduction to VLSI Testing*", Prentice Hall, 1st Illustrated Edition, 1998.

ADDITIONAL LEARNING RESOURCES

http://www2.eng.cam.ac.uk/~dmh/4b7/resource/section16.htm

https://nptel.ac.in/courses/106103016/21

https://nptel.ac.in/courses/106105161/54

M. Tech.– I Semester

(19MT15707) FPGA ARCHITECTURES

(Program Elective-2)

(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Digital Logic Design and VLSI Design at UG Level.

COURSE DESCRIPTION:

Evolution of Programmable Devices, Xilinx, Actel, Altera FPGAs, Logic Synthesis, Technology Mapping, Finite State Machines, Realizations of SM Charts, One Hot Method, System level Design, Device Applications-Fast Bus Controller, FIFO Controller & Intelligent I/O Subsystem

COURSE OBJECTIVES:

CEO1: To impart knowledge in architectures and applications of various families of CPLDs and FPGAs.
CEO2: To develop skills in design, analysis and problem solving for implementation and verification of functions in CPLDs/FPGAs.
CEO3: Apply knowledge and skills for performance analysis in the design of FSMs.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze the architectures of programmable logic devices and technology mapping issues in CPLDs and FPGAs.
CO2. Analyze various Finite state machine charts and its architectures to evaluate the performance of VLSI systems.
CO3. Understand the applications of FPGA in communications, speech processing, Image and video processing.

DETAILED SYLLABUS:

Unit - I: Introduction to Programmable Logic and FPGAs (Hours: 08)
Evolution of Programmable Devices, CPLD Altera Series Max 5000, MAX 7000 Series. Field Programmable Gate Arrays –Design Flow, Placement , Routing Architecture. Altera FPGAs. Advanced Micro Devices (AMD) FPGA. Applications of FPGAs.

Unit - II: (Hours: 09)
Xillinx and Actel FPGAs :
Case Studies – Xilinx XC2000, XilinxXC3000, Xilinx 4000 FPGAS. Actel FPGAs- Actel ACT1, Actel ACT2, Actel ACT3.
Technology Mapping for FPGAs: Logic Synthesis. Lookup Table Technology, Mapping Multiplexer Technology Mapping- The Proserphine Technology Mapper, Multiplexers Technology Mapping in Mis pga, A map and XA map Technology Mappers.

Unit - III: Finite State Machine **(Hours: 09)**

Finite State Machines, State Transition Table, State Assignment for FPGAs, Hazards and One Hot Encoding. Mustang. State Machine Charts, Derivations of State Machine Charges, Realization of State Machine Charts.

Unit - IV: FSM Architectures and System Level Design **(Hours: 10)**

Architectures Centered Around Non Registered PLDs, State Machine Designs Centered Around Shift Registers, One – Hot Design Method, Use of ASMs in One Hot Design, Application of One Hot Method. System Level Design – Controller, Data Path and Functional Partition.

Unit - V: Device Applications **(Hours: 09)**

MAX 5000 Timing, Using Expanders to Build Registered Logic in MAX EPLDs, Simulating Internal Buses in General Purpose EPLDs, Fast Bus Controllers with EPM5016, Micro Channel Bus Master and SDP Logic with the EPM5032 EPLD, FIFO Controller Using an EPM7096, Integrating an Intelligent I/O Subsystem with a Single EPM5130 EPLD.

Total Hours: 45

TEXT BOOKS:

1. S.Brown, R.Francis, J.Rose, Z.Vransic, "*Field Programmable Gate Array*", Kluwer Publication, 1992.
2. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall (PTE), 1994
3. Richard Tinder, "*Engineering Digital Design*", Academic Press, 2nd Edition, 2000.

REFERENCE BOOKS:

1. Charles H. Roth, Jr, "*Fundamentals of Logic Design*", Cengage Learning, 5th Edition, 2004.
2. S.Trimberger, Edr., "*Field Programmable Gate Array Technology*", Kluwer Academic Publications, 1994.

M. Tech. - I Semester
(19MT15708) LOW POWER CMOS VLSI DESIGN
(Program Elective - 2)
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on VLSI Design at UG Level

COURSE DESCRIPTION:

Need for low power VLSI chips, Sources of Power dissipation in MOS & CMOS Devices, Power Estimation, Synthesis of low power VLSI Circuits, Design of low power VLSI Circuits, Low power Memory Architectures, Energy recovery Circuits, Software design of low power VLSI Circuits.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in low power CMOS Circuits.
CEO2: To develop skills in design, analysis and problem solving related to high performance and low power devices.
CEO3: Apply knowledge and skills pertaining to low voltage CMOS circuit design for for wide range of IC applications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze the various power dissipation effects and estimation methods in CMOS VLSI Circuits to improve the performance characteristics of digital systems.
CO2. Understand the various design styles and synthesis of low power and low voltage CMOS VLSI circuits.
CO3. Analyze the various low power Static RAM architectures in design and development of Ultra Low power Integrated Circuits.
CO4. Apply energy recovery techniques to evaluate the performance of low power VLSI Circuits for scientific research in design and development of digital systems.

DETAILED SYLLABUS:

Unit –I **(Hours: 07)**
Power Dissipation in CMOS VLSI design: Need for low power VLSI chips, Sources of Power dissipation, Power dissipation in MOS & CMOS Devices, Limitations of low Power design.

Unit –II **(Hours: 08)**
Power Estimation: Modeling of Signals, Signal Probability Calculation, Probabilistic Techniques for Signal activity Estimation, Statistical Techniques, Estimation of Glitching Power, Sensitivity Analysis, Power Estimation using input vector Compaction, Estimation of Maximum Power.

Unit-III **(Hours: 10)**
Synthesis for Low Power: Behavioral Level Transforms, Logic Level optimization of low power, Circuit level.
Design and Test of Low Voltage CMOS Circuits: Circuit Design Style, Leakage current in Deep Sub micrometer Transistors, Low voltage Circuit Design Techniques, Multiple Supply Voltages.

Unit-IV **(Hours: 10)**

Low Power Static RAM Architectures: Organization of Static RAM, MOS Static RAM Memory Cell, Banked Organization of SRAMs, Reducing Voltage Swing in Bit lines, Reducing Power in Sense Amplifier Circuits.

Unit-V **(Hours: 10)**

Low Energy Computing using Energy Recovery Techniques: Energy Recovery Circuit Design, Designs with partially Reversible logic, Supply Clock Generation.

Software design for low power: Sources of software power dissipation, software power estimation, Software power estimation, Co-design for low power.

Total Hours: 45

TEXT BOOK:

1. Kaushik Roy, Sharat Prasad, "*Low-Power CMOS VLSI Circuit Design*" Wiley Student Edition, 2000.

REFERENCE BOOK:

1. Kiat-Seng Yeo, Samir S.Rofail and Wang-Ling Goh, "*CMOS/BiCMOS ULSI: Low power, Low Voltage* ", Pearson education, 2002.

M. Tech. - I Semester
(19MT15709) MIXED SIGNAL DESIGN
(Program Elective-2)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Analog Design at UG Level.

COURSE DESCRIPTION:

Switched capacitor circuits - analysis and application; Design and characterization of Phase locked loops; Data converters – types; Design for different sampling rates.

COURSE OBJECTIVES:

CEO1: To impart basic and advanced knowledge in Mixed signal design.
CEO2: To develop skills in design, analysis, problem solving and research in Switched capacitor circuits, phase locked loop and data converters

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Design switched capacitor circuits, phase locked loops and charge pump based PLL to improve Performance characteristics of mixed signal systems.
CO2. Design ADC and DAC to increase the Data Rate for signal processing and Communication applications.
CO3. Develop high speed modulators, interpolating & decimating filters for analog and digital communications.

DETAILED SYLLABUS:

Unit - I: Switched Capacitor Circuits (Hours: 12)
Introduction to analog VLSI and mixed signal issues in CMOS technologies, Trade-offs in mixed signal design, Introduction to Switched Capacitor circuits - basic building blocks, Operation and Analysis, Non-idealeffects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, Biquad filters.

Unit - II: Phase Locked Loop (PLL) (Hours: 08)
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

Unit - III: Data Converter Fundamentals (Hours: 13)
DC and dynamic specifications, Quantization noise, performance limitations, Nyquist rate D/A converters - Decoder based Converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

Unit - IV: Nyquist Rate A/D Converters (Hours: 05)
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D Converters, Folding A/D converters, Pipelined A/D converters, Time-Interleaved Converters.

Unit - V: Oversampling Converters (Hours: 07)
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A.

Total Hours: 45

TEXT BOOKS:

1. David A. Johns,Ken Martin, "*Analog Integrated Circuit Design*", Wiley Student Edition, 1997.
2. Behzad Razavi, "*Design of Analog CMOS Integrated Circuits*", Tata McGraw Hill Edition, 2001.
3. Philip E. Allen and Douglas R. Holberg, "*CMOS Analog Circuit Design"*, Oxford University Press, 3rd Edition, 2012.

REFERENCE BOOKS:

1. Rudy Van De Plassche, "*CMOS Integrated Analog-to-Digital and Digital-to-Analog converters"*, Springer US, 2nd Illustrated Edition, 2003.
2. Richard Schreier, "*Understanding Delta-Sigma Data converters*", Wiley Interscience, 1st Edition, 2004.
3. R. Jacob Baker, "*CMOS Mixed-Signal Circuit Design*", John Wiley & Sons, 2002.

M. Tech. - I Semester
(19MT10708) RESEARCH METHODOLOGY AND IPR

(Common to all M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	2	-	-	2

PRE REQUISITES:

COURSE DESCRIPTION:

Overview of research; research problem and design; various research designs; Data collection methods; Statistical methods for research;Interpretation& drafting reports and Intellectual property rights.

COURSE OBJECTIVES:

CEO1: To impart knowledge on research methodology and subsequent process involved for successful accomplishment of the research.
CEO2: To impart knowledge on intellectual property rights and subsequent process involved in filing patents and trade mark registration process.
CEO3: To inculcate attitude of reflective learning and contribute to the society through fruitful research.

COURSE OUTCOMES:

On successful completion of the course, students will be able to:

CO1. Apply the conceptual knowledge of research methodology to formulate the hypothesis, data collection and processing, analyzing the data using statistical methods, interpret the observations and communicating the novel findings through a research report.
CO2. Practice ethics and have responsibility towards society throughout the research process and indulge in continuous learning process.
CO3. Apply the conceptual knowledge of intellectual property rights for filing patents and trade mark registration process.

DETAILED SYLLABUS:

Unit-I: Introduction to Research Methodology (Hours: 07)
Objectives and Motivation of Research, Types of Research, Defining and Formulating the Research Problem; Features of research design, Different Research Designs; Different Methods of Data Collection, Data preparation and Processing.

Unit-II: Data Analysis and Hypothesis Testing (Hours: 09)
ANOVA; Principles of least squares-Regression and correlation; Normal Distribution-Properties of Normal Distribution; Testing of Hypothesis – Hypothesis Testing Procedure, Types of errors, t-Distribution, Chi-Square Test as a Test of Goodness of Fit.

Unit-III: Interpretation and Report Writing (Hours: 04)
Interpretation – Need, Techniques and Precautions; Report Writing – Significance, Different Steps, Layout, Types of reports,Mechanics of Writing a Research Report, Precautions in Writing Reports; Research ethics.

Unit-IV: Introduction to Intellectual property and Trade Marks (Hours: 07)
Importance of intellectual property rights; types of intellectual property, international organizations; Purpose and function of trademarks, acquisition of trade mark rights, protectable matter, selecting and evaluating trade mark, trade mark registration processes.

Unit-V: Law of Copyrights (Hours: 08)
Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.
Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer
New Developments in IPR: Administration of Patent System.

Total Hours: 35

TEXT BOOKS:

1. C.R. Kothari, *Research Methodology: Methods and Techniques*, 2nd revised edition, New Age International Publishers, New Delhi, 2004.
2. Deborah, E. Bouchoux, *Intellectual property right*, 5th edition, Cengage learning, 2017.

REFERENCE BOOKS:

1. R. Panneerselvam, *Research Methodology*, PHI learning Pvt. Ltd., 2009.
2. Prabuddha Ganguli, *Intellectual property right - Unleashing the knowledge economy*, Tata McGraw Hill Publishing Company Ltd, 2001.

M. Tech. – I Semester
(19MT15731) ANALOG CMOS VLSI DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

A Course on electronic circuit analysis and VLSI Design at UG Level.

COURSE DESCRIPTION:

Single Stage CMOS Amplifiers, Cascode Amplifiers, Feedback Amplifiers, Operational Amplifiers, Gain Boosting and Frequency Compensation Techniques, Bandgap References, Switched Capacitor Circuits, Sampling Switches, Ring Oscillator, PLL.

COURSE OBJECTIVES:

CEO1: To impart knowledge on modeling Analog circuits.
CEO2: To develop and apply techniques for boosting gain and compensating frequency.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Design and Develop Feedback Amplifiers and Operational Amplifiers.
CO2. Apply suitable compensation techniques to design CMOS circuits.
CO3. Analyze various Bandgap references to compensate the issues in design specifications.
CO4. Develop switched capacitor circuits for various filter designs.
CO5. Work individually and in groups to solve problems with effective communication.

List of Exercises /Experiments: (10-12 Exercises/Experiments)

1. Model the single stage amplifiers (Common Source Amplifier, Common Drain Amplifier, Common Gate Amplifier) using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.

2. Model the Differential Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.

3. Model the Cascode Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Output Resistance, Power Dissipation, etc.

4. Model the Operational amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like gain, Output Resistance, Power Dissipation, etc.

5. Model the Feedback Amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like gain, Output Resistance, Power Dissipation, etc.

6. Model and apply the gain boosting techniques to CMOS amplifiers using SPICE Language, develop their schematic and layout to evaluate the Parameters like Gain, Power Dissipation, etc.

7. Model and apply the frequency compensation techniques to CMOS amplifiers using SPICE Language, develop their schematic and layout to obtain their frequency response.

8. Model Bandgap Reference Circuits by using SPICE Language, develop their schematic and layout to obtain their Characteristics.

9. Model Sampling Switches using SPICE Language, develop their schematic and layout to obtain their characteristics.

10. Model Switched Capacitor Amplifier and Integrator using SPICE Language, develop their schematic and layout to obtain their characteristics.

11. Model Ring Oscillator using SPICE Language, develop their schematic and layout to obtain their characteristics.

12. Model Phase Locked Loop using SPICE Language, develop their schematic and layout to obtain their characteristics.

13. Mini Projects (MPs):
    Form a group of maximum 2 members as a team and assign mini projects related to Development of compensation techniques and design of alternative subsystem designs.

REFERENCE BOOKS/LABORATORY MANUALS

1. ECE Department *Analog CMOS VLSI Design* Lab Manual.
2. Behzad Razavi, "*Design of Analog CMOS Integrated Circuit*", Tata McGraw-Hill, 14th Reprint 2008.

SOFTWARE/TOOLS USED:

Cadence/synopsys/mentor graphics

ADDITIONAL LEARNING RESOURCES

1. https://nptel.ac.in/courses/117101105/

M. Tech. – I Semester
(19MT15732) DIGITAL CMOS VLSI DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

A Course on electronic circuit analysis and VLSI Design at UG Level.

COURSE DESCRIPTION:

Alternate CMOS combinational and sequential Logic Circuits, Clock Generation, Skew and Synchronization, Logical Effort, Memories, Adders, Multipliers, Shifters, ALU, Arithmetic Processor, Pipelining.

COURSE OBJECTIVES:

CEO1: To impart knowledge on modeling Digital CMOS circuits.
CEO2: To develop programming skills to solve problems in designing subsystems or processors.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Analyze CMOS logic styles for combinational and sequential circuits.
CO2. Design and develop alternative subsystems for the design of a processor.
CO3. Design CMOS memories for high speed networks.
CO4. Work individually and in groups to solve problems with effective communication.

List of Exercises/Experiments: (10-12 Exercises/Experiments)

1. Model alternate CMOS Logic styles for Logic Gates using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

2. Model static and dynamic CMOS Logic for sequential circuits using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

3. Model clock generation circuits for synchronization to avoid skew using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

4. Model the effect of Logical Effort on CMOS Logic using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

5. Model SRAM and DRAM using SPICE and assess the parameters like power dissipation, delay and output waveform characteristics.

6. Model n-bit Adder using Hardware Description Language and perform its functional simulation.

7. Model n-bit Modified Booth Multiplier using Hardware Description Language and perform its functional simulation.

8. Model n-bit Barrel Shifter using Hardware Description Language and perform its functional simulation.

9. Model n-bit Arithmetic and Logic Unit using Hardware Description Language and perform its functional simulation.

10. Design Read Only Memory (ROM), Random Access Memory (RAM), Model them using Hardware Description Language and perform its functional simulation.

11. Design a 4-bit Arithmetic Processor with and without pipelining, Model it using Hardware Description Language and perform its functional simulation.

12. Implementation of Experiments 6 to 11 on FPGA/ CPLD.

13. Mini Projects (MPs):
    Form a group of maximum 2 members as a team and assign mini projects related to Development of compensation techniques and design of alternative subsystem designs.

REFERENCE BOOKS/LABORATORY MANUALS

1. ECE Department Digital CMOS VLSI Design Lab Manual.
2. Jan M Rabaey, "Digital Integrated Circuits", Pearson Education, 2nd Edition, 2003.

SOFTWARE/TOOLS USED:

Cadence/synopsys/mentor graphics/ Xilinx

ADDITIONAL LEARNING RESOURCES

1. https://onlinecourses.nptel.ac.in/noc19_ee25
2. https://nptel.ac.in/courses/117101105/

M. Tech. - I Semester
(19MT1AC01) TECHNICAL REPORT WRITING
(Audit Course)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	*2*	-	-	-

PRE-REQUISITES: -

COURSE DESCRIPTION:

Introduction; Process of writing; Style of writing; Referencing; Presentation.

COURSE OBJECTIVES:

CEO1: To impart the knowledge of structure and layout of Business and Technical Reports.
CEO2: To learn styles and techniques of description for effective reports.
CEO3: To develop the ability to understand & interpret the writing techniques for effective communication in written documents.

COURSE OUTCOMES:

After successful completion of this course, the students will be able to:

CO1. Demonstrate knowledge of Technical Report Writing by examining kinds of reports and structure with scientific attitude.
CO2. Apply the techniques in preparing effective reports by examining Techniques of Description, Describing Machines and Mechanisms and Describing Processes.
CO3. Communicate effectively through writing technical reports by demonstrating the knowledge of Industry Reports, Survey Reports, Interpretive Report and Letter Report.

DETAILED SYLLABUS:

Unit I - **Introduction** **(Hours: 06)**
Introduction to Technical Report - Types of Reports - Planning Technical Report Writing - Components of a Technical Report - Report Writing in Science and Technology - Selecting and Preparing a 'Title' - Language Use in Report Writing.

Unit II - **Process of Writing** **(Hours: 05)**
Writing the 'Introduction' - Writing the 'Materials and Methods' – Writing the Findings/Results'- Writing the 'Discussion' - Preparing and using 'Tables'.

Unit III - **Style of Writing** **(Hours: 06)**
Preparing and using Effective 'Graphs' - Citing and Arranging References—I - Citing and Arranging References —II - Writing for Publication in a Scientific Journal.

Unit IV - **Referencing** **(Hours: 09)**
Literature citations - Introductory remarks on literature citations - Reasons for literature citations – Bibliographical data according to ISO - Citations in the text - Copyright and copyright laws - The text of the Technical Report - Using word processing and desktop publishing (DTP) systems - Document or page layout and hints on editing - Typographic details - Cross-references.

Unit IV - **Presentation** **(Hours: 04)**
Giving the presentation - Appropriate pointing - Dealing with intermediate questions - Review and analysis of the presentation - Rhetoric tips from A to Z.

Total Hours: 30

TEXT BOOKS:

1. R C Sharma – Krishna Mohan, *"Business Correspondence and Report Writing,"* Tata McGraw-Hill Publishing Company Limited, New Delhi, Third Edition, 2005 (reprint).
2. Patrick Forsyth*, "How to Write Reports and Proposals",* THE SUNDAY TIMES (Kogan Page), New Delhi, Revised Second Edition, 2010.

REFERENCE BOOKS:

1. John Seely, "*The Oxford Writing & Speaking"*, Oxford University Press, Indian Edition.
2. Anne Eisenberg, *"A Beginner's Guide to Technical Communication"*, McGraw Hill Education (India) Private Limited, New Delhi, 2013.

ADDITIONAL LEARNING RESOURCES

1. http://www.resumania.com/arcindex.html
2. http://www.aresearchguide.com/writing-a-technical-report.html
3. http://www.sussex.ac.uk/ei/internal/forstudents/engineeringdesign/studyguides/tec report writing

M. Tech. – II Semester
(19MT25701) NANO MATERIALS AND NANOTECHNOLOGY

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Basic Engineering Physics, Basic Engineering Chemistry and Electronic Devices at UG Level.

COURSE DESCRIPTION:

Nanostructures – Classification and Peculiarities, Characterization and Properties of Nanomaterials, Micro Electro-Mechanical Systems (MEMS) & Nano Electro-Mechanical Systems (NEMS), Carbon Nanotubes (CNT) – Properties and Synthesis, Interdisciplinary Applications of Nanomaterials.

COURSE OBJECTIVES:

CEO1: To relate unique properties of nanomaterials to the reduce dimensionality of the material.
CEO2: To impart skills on nanostructures fabrication.
CEO3: To provide knowledge on nanomaterials and implication of health and safety related to nanomaterials.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand the peculiarities of Nanostructured materials, their characterization and properties to solve structural, mechanical and electrical problems in manufacturing Nanostructures.
CO2. Use IC Fabrication techniques to manufacture Micro Electro-Mechanical Systems (MEMS) and Nano Electro-Mechanical Systems (NEMS).
CO3. Understand carbon nanotube properties and its synthesis for various applications.
CO4. Apply the properties of nanomaterials by fixing the boundaries in system development in multidisciplinary areas like Automobiles, Biomedical, Agriculture.

DETAILED SYLLABUS:

Unit - I: Nanostructures and Peculiarities of Nanostructured Materials (Hours: 09)

Gleiter's classification of nanostructured materials, Classification of nanostructures by dimensionality, Concept of "surface form engineering" in nanomaterial science, Extended internal surface, Increasing of surface energy and tension, Grain boundaries, Instability of 3D0 NSM due to grain growth.

Unit – II: Characterization and Properties of Nanomaterials (Hours: 11)

Structural Characterization: X-ray diffraction (XRD),Scanning electron microscopy (SEM), Transmission electron microscopy (TEM), Chemical Characterization: Optical spectroscopy, Electron spectroscopy, Ionic spectrometry, Physical Properties of Nanomaterials: Melting points and lattice constants, Mechanical properties, Optical properties Electrical conductivity.

Unit – III: Micro Electro-Mechanical Systems (MEMS) and Nano Electro-Mechanical Systems (NEMS) (Hours: 08)

Introduction, Fabrication of MEMS and NEMS, Surface micromachining, Bulk Micromachining, Fabrication stages, Deposition, Patterning, Etching.

Unit – IV: Carbon Nanotubes (CNT) – Properties and Synthesis (Hours: 09)
Dimensions, Chirality, Material Properties, Mechanical Properties, Electrical Properties, Optical Properties, Thermal Properties, Nanotube Growth Methods, Chemical Vapor Deposition, Thermal Chemical Vapor Deposition, Other Growth Methods: Arc Discharge, Laser Ablation, Applications

Unit – V: Interdisciplinary Arena of Nanomaterials (Hours: 08)
Molecular Electronics and Nanoelectronics, Nanobots, Biological Applications of Nanoparticles, Catalysis by Gold Nanoparticles, Band Gap Engineered Quantum Devices, Nanomechanics Carbon Nanotube Emitters, Photoelectrochemical Cells, Photonic Crystals and Plasmon Waveguides

Total Hours: 45

TEXT BOOKS:

1. A I Gusev and A ARempel, "*Nanocrystalline Materials*", Cambridge International Science Publishing, 1st Indian edition, 2008.
2. Guozhong Cao and Ying Wang, "*Nanostructures and Nanomaterials: Synthesis, Properties, and Applications",* Imperial College Press, 2004.

REFERENCE BOOKS:

1. Bhushan, Bharat, "*Springer Handbook of Nanotechnology*", 2nd edition, 2006.
2. Pokropivny, Vladimir, Rynno Lohmus, Irina Hussainova, Alex Pokropivny, and Sergey Vlassov, "*Introduction to nanomaterials and nanotechnology*", Tartu, Estonia: Tartu University Press, 2007.
3. Kamal K. Kar, "*Carbon Nanotubes: Synthesis, Characterization and Applications",* Research Publishing Services, 1st edition, 2011.

ADDITIONAL LEARNING RESOURCES

1. *Introduction to Nanotechnology*, nanohub.org
2. https://nptel.ac.in/courses/103103033/module9/lecture1.pdf

M. Tech. – II Semester
(19MT25702) PHYSICAL DESIGN AUTOMATION
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on VLSI Design and Digital IC Design at UG Level.

COURSE DESCRIPTION:

Basics of VLSI design; Layout optimization; Simulation and synthesis; Physical design of FPGAs and MCMs.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in Physical Design Automation for Backend Design and Tape out of ICs.
CEO2: To develop and apply skills in design, analysis and solving problems in layouts of Backend Design.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand the various VLSI Design Methodologies and layout compaction algorithms for the development of optimized designs.
CO2. Analyze various levels of simulation and logic synthesis to model hardware.
CO3. Apply Automation algorithms for physical design cycles of FPGAs and MCMs.

DETAILED SYLLABUS:

Unit – I: Introduction To VLSI Design Methodologies (Hours: 08)
Introduction to VLSI Design automation tools, Introduction to algorithmic graph theory, Computational Complexity, Tractable and Intractable problems, Combinational optimization.

Unit – II: Layout Compaction (Hours: 09)
Design rules, problem formulation, algorithms for constraint graph compaction, placement & partitioning algorithms. Floor planning concepts- shape functions and floor plan sizing, types of routing problems.

Unit - III: Simulation And Synthesis (Hours: 08)
Gate Level Modeling and Simulation, Switch Level Modeling and Simulation. Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

Unit – IV: High Level Synthesis (Hours: 10)
Hardware modeling, internal representation of the input algorithm, allocation, assignment and scheduling algorithms, ASAP scheduling, Mobility based scheduling, list scheduling & force-directed scheduling.

Unit–V: Physical Design Automation of FPGAs and MCMs (Hours: 10)
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models, MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Routing and Programmable MCMs.

Total Hours: 45

TEXTBOOKS:

1. S.H.Gerez, "*Algorithms for VLSI Design Automation*", John wiley & Sons Pvt. Ltd, 2nd Edition 1999.
2. Naveed Sherwani, "*Algorithms for VLSI Physical Design Automation*", Springer International Edition, 3rd edition, 2005.

REFERENCE BOOKS:

1. Hill & Peterson, "*Computer Aided Logical Design with Emphasis on VLSI*", John Wiley & Sons Pvt. Ltd, 4th edition, 1993.
2. Wayne Wolf, "*Modern VLSI Design Systems on silicon*", Pearson Education Asia, 2nd Edition, 1998.

ADDITIONAL LEARNING RESOURCES

https://nptel.ac.in/courses/106105161/

M. Tech. – II Semester
(19MT25703) CO DESIGN
(Program Elective - 3)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Computer Architecture, Digital Design, Software Design, and Embedded Systems at UG Level.

COURSE DESCRIPTION:

Issues and Algorithms in CO- Design; Prototyping and its Emulation on Target Architectures; Compilation Techniques; Design Specification; Verification Tools for Embedded Processor Architectures; System- Level Languages with its Specification and Design.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in complex computer system designs.
CEO2: To develop analysis, problem solving, design, simulation, interdisciplinary, communication and application skills in Hardware software co-design practices.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand the issues in Co-design and analyze Co-Synthesis Algorithms for Co-Design Architectures.
CO2. Analyze Prototyping and emulation for specialized target architectures for system design.
CO3. Select appropriate architectures in designing data-dominated and control-dominated embedded systems.
CO4. Use compilation techniques and tools for embedded processor architectures with an understanding of practical considerations and perform verification of co-design computational models.
CO5. Apply language support for system level specification, co-simulation design and partitioning concepts in Cosyma and Lycos systems

DETAILED SYLLABUS

Unit–I: (Hours: 11)
CO- Design Issues: Co-design Models, Architectures, Languages, a Generic Co-design Methodology
Co-Synthesis Algorithms: Architectural Models, Hardware/Software Partitioning, Distributed System Co-Synthesis

Unit – II: (Hours: 07)
Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping
Target Architectures- I: Architecture Specialization techniques, System Communication infrastructure

Unit -III: Target Architectures – II: (Hours: 07)
Target Architecture and Application System classes, Architecture for control dominated systems- 8051. Architectures for High performance control, Architecture for Data dominated systems- ADSP21060, TMS320C.

Unit – IV: **(Hours: 09)**

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, Practical consideration in a compiler development environment.

Design Specification and Verification: The co-design computational model, coordinating concurrent computations, interfacing components, Verification- Design verification and implementation verification, verification tools and interface verification.

Unit–V: **(Hours: 11)**

Languages for System- Level Specification and Design: System Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specifications and Multi Language Co-simulation- Concepts for Multi-language design , Co-simulation models.

The Cosyma Systems: Overview, Architecture- design flow and user interaction. Partitioning, Synthesis

Lycos System: Introduction, Partitioning and Design Space Exploration

Total Hours: 45

TEXT BOOK:

1. Jorgen Staunstrup, Wayne Wolf, "*Hardware / software co- design Principles and Practice"*, Springer, 2009.

REFERENCE BOOK:

1. Felice Balarine, "*Hardware-Software Co-Design of Embedded Systems: The Polis Approach"*, Springer, 1991.

ADDITIONAL LEARNING RESOURCES

https://www.tec.ee.ethz.ch/education/lectures/hardware-software-codesign.html
https://www.coursera.org/learn/introduction-embedded-systems
https://nptel.ac.in/courses/108102045/30
https://ieeexplore.ieee.org/document/7525779

M. Tech. - II Semester
(19MT25704) MEMORY TECHNOLOGIES
(Program Elective - 3)
(Common to VLSI & DECS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Digital Electronics and VLSI design at UG Level

COURSE DESCRIPTION:

Random access memory Technology; Non-Volatile memory designs; Reliability and Radiation effects of semiconductor memory; Packaging technologies, Fault modeling and Testing of memory.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge on various memory Technologies.
CEO2: To develop skills in design and analysis of different memory architectures and Packaging.
CEO3: Apply knowledge and skills to develop optimized memory design to solve real time problems.

COURSE OUTCOMES:

On successful completion of the course, students will be able to

CO1. Understand various Random Access Memory Technologies, Non-Volatile Memory Designs and Technologies for optimized memory design.
CO2. Analyze the reliability and radiation issues of semiconductor memories for different memory Architectures.
CO3. Apply advanced memory and high packaging technologies in memory optimization.
CO4. Use the various memory fault models and appropriate testing Techniques to improve the performance of systems.

DETAILED SYLLABUS:

Unit – I: Random Access Memory Technologies (Hours: 11)
Static Random Access Memories (SRAMs): Basic SRAM Architecture and Cell Structures, High performance SRAMs, Advanced SRAM Architectures , BiCMOS SRAMs, Low-Voltage SRAMs ,SOI SRAMs, Specialty SRAMs.
Dynamic Random Access Memories (DRAMs): DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs, Cache DRAM, Virtual Channel Memory (VCM) DRAMs, Multilevel Storage DRAMs , SOI DRAMs , Gigabit DRAM Scaling Issues and Architectures, Advanced DRAM design and Architecture, Application Specific DRAMs.

Unit – II: Non-Volatile Memory Designs and Technologies (Hours: 08)
Masked Read-Only Memories (ROMs), Programmable Read-Only Memories (PROMs), Non-volatile memory advances, Floating Gate Cell Theory and Operations, Erasable (UV) - Programmable Road-Only Memories (EPROMs), Electrically Erasable PROMs (EEPROMs), Flash Memories, Multilevel Nonvolatile Memories.

Unit – III: Semiconductor Memory Reliability and Radiation Effects (Hours: 09)
Reliability: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory Reliability, Reliability Modeling, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification.

Radiation: Radiation Effects, Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics, Radiation hardness assurance.

Unit – IV: Advanced Memory and High-Density Packing Technologies **(Hours: 09)**

Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto resistive Random Access Memory, Experimental Memory Devices. Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory Cards, High Density Memory Packaging Future Directions.

Unit – V: Memory Fault Modeling and Testing **(Hours: 08)**

RAM Fault Modeling, Electrical Testing, RAM Peusdo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing, Memory error detection and correction Techniques.

Total Hours: 45

TEXT BOOKS:

1. Ashok K Sharma, *"Advanced Semiconductor Memories: Architectures, Designs and Applications"*, Wiley Interscience, 2003.
2. Ashok K Sharma,"*Semiconductor Memories:Technology*", Testing & Reliability, PHI, 2012.

REFERENCE BOOKS:

1. Kiyoo Itoh, "*VLSI memory chip design*", Springer International Edition, 2001.
2. Luecke Mize Carr, "*Semiconductor Memory design and Application*", Mc-Graw Hill, 1973

ADDITIONAL LEARNING RESOURCES

https://researcher.watson.ibm.com/researcher/view_group.php?id=7956
https://www.electronics-notes.com/articles/electronic_components/semiconductor-ic-memory/memory-types-technologies.php
https://nptel.ac.in/courses/117106111/24
https://nptel.ac.in/courses/106105033/32
https://nptel.ac.in/courses/106104122/30
https://nptel.ac.in/courses/117101058/28

M. Tech. - II SEMESTER
(19MT25705) SYSTEM-ON-CHIP DESIGN
(Program Elective – 3)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Embedded systems and VLSI design.

COURSE DESCRIPTION:

System on Chip Design Process; System level Design Issues; Test Strategies; Macro Design and Verification; Reusable Macros; System on Chip Verification; Communication Architectures for SoCs.

COURSE OBJECTIVES:

CEO1: To impart knowledge in understanding the concepts of Design, Verification and Communication Architectures for SoCs.
CEO2: To develop analytical, usage of techniques, research and design skills in evaluating and verifying designs for SoC architectures.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand various SoC Design aspects and issues in low power and high speed implementations.
CO2. Analyze the Macro Design Process to solve issues in usage of hard macros and develop resusable macros for system integration.
CO3. Analyze verification methods at system level, block level and Hardware/Software Co-verification to reduce the test time.
CO4. Apply various communication architectures to design energy efficient systems.

DETAILED SYLLABUS:

Unit-I: System on Chip Design Process (Hours: 08)
A canonical SoC Design, SoC Design flow- waterfall vs spiral, top down vs Bottom up. Specification requirement, Types of Specification, System Design process, System level design issues - Soft IP Vs Hard IP, Design for timing closure - Logic design issues, Verification strategy, Onchip buses and interfaces, Design for Low Power, Manufacturing test strategies.

Unit-II: Macro Design Process (Hours: 07)
Overview of IP Design, planning and Specification, Macro Design and Verification, Soft Macro Productization, Developing hard macros - Design issues for hard macros, Model Development for Hard Macros. System Integration with reusable Macros.

Unit-III: SoC Verification - I (Hours: 12)
Technology Challenges, Verification technology options, Verification methodology, Testbench Creation, Testbench Migration, Verification languages, Verification IP Reuse, Verification approaches, Verification and Device Test, Verification plans, Bluetooth SoC.
System level verification – System Design, System Verification.
Block level verification – IP Blocks, Block Details of Bluetooth SoC, Lint Checking, Formal Model Checking, Functional Verification/Simulation, Protocol Checking, Directed Random Testing, Code Coverage Analysis.

Unit-IV: SoC Verification - II (Hours:12)
Hardware/Software Co-verification- HW/SW Co-verification Environment, Emulation, soft or virtual Prototypes, Co-verification, UART Co-verification, Rapid Prototype Systems, Software Testing. Static netlist verification, Physical Verification and Design Signoff, Introduction to VMM (Verification Methodology Manual), OVM(Open Verification Methodology) and UVM (Universal Verification Methodology).

Unit-V: Design of Communication Architectures for SoCs (Hours: 06)
On chip communication architectures, System level analysis for designing communication, Design space exploration, Adaptive communication architectures - Communication architecture tuners. Communication architectures for energy/battery efficient systems. Introduction to bus functional models and bus functional model based verification.

Total Hours: 45

TEXT BOOKS:

1. Michael Keating, Pierre Bricaud, "*Reuse Methodology manual for System On A Chip Designs*", Kluwer Academic Publishers, 3rdEdition, 2002.
2. Prakash Rashinkar, Peter Paterson and Leena Singh, "*SoC Verification Methodology and Techniques"*, Kluwer Academic Publishers, 2002.
3. A.A. Jerraya, W.Wolf, "*Multiprocessor Systems-on-chips*", M K Publishers, 2005.

REFERENCE BOOKS:

1. William K. Lam, "*Hardware Design Verification: Simulation and Formal Method based Approaches",* Prentice Hall, 1st Edition, 2005.
2. Farzed Nekoogar, Faranak Nekoogar, *"From ASICs to SOCs: A Practical Approach*", Prentice Hall PTR, 2003.

ADDITIONAL LEARNING RESOURCES

https://nptel.ac.in/courses/108102045/10
https://nptel.ac.in/courses/106102181/2
https://nptel.ac.in/courses/108102045/

M. Tech. – II Semester
(19MT25706) COMMUNICATION BUSES AND INTERFACES
(Program Elective – 4)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Computer Organization and Microprocessor & Microcontrollers.

COURSE DESCRIPTION:

Serial Busses, RS232 – Limitations and Applications, CAN Protocol, USB – Types, Architecture, Serial Communication Protocol using Physical Medium.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in design of Communication protocols and interfaces.
CEO2: To develop skills in design, analysis and problem solving for high speed data transfer among communication devices.
CEO3: To apply knowledge and skills of physical interconnects and standards for the development of new communication busses and physical interfaces.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand the features of various serial protocols for high speed data communication between ICs in a Board.
CO2. Analyze the limitations of RS232 to solve the problems in various communicating devices.
CO3. Develop the architecture of Controller Area Network for Application layer communication.
CO4. Apply PCIe hardware Protocol for high speed communication between compatible devices.
CO5. Apply appropriate serial communication protocols and USB transfer types for high performance communication bus.

DETAILED SYLLABUS:

Unit – I: Serial Bus **(Hours: 06)**
Physical interface, Data and Control signals, features

Unit – II: Introduction to Serial standards **(Hours: 08)**
Limitations and applications of RS232, RS485, I2C, SPI

Unit - III: Controller Area Network **(Hours: 10)**
CAN - Architecture, Data transmission, Layers, Frame formats, applications

Unit – IV: Introduction To PCIe **(Hours: 08)**
PCIe - Revisions, Configuration space, Hardware protocols, applications

Unit – V: Universal Serial Bus **(Hours: 13)**
USB - Transfer types, enumeration, Descriptor types and contents, Device driver.
Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

Total Hours: 45

TEXT BOOKS:

1. Jan Axelson, "*Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems"*, Lakeview Research, 2nd Edition.
2. Marco Di Natale, Haibo Zeng, Paolo Giusto, Arkadeb Ghosal, "*Understanding and Using the Controller Area Network Communication Protocol: Theory and Practice*" Springer Science & Business Media, 2012.

REFERENCE BOOKS:

1. Wilfried Voss, "*A Comprehensible Guide to Controller Area Network*", Copperhill Media Corporation, 2nd Edition, 2005.
2. Jan Axelson, "*USB Complete*", Penram Publications.
3. Mike Jackson, Ravi Budruk, "*PCI Express Technology*", Mindshare Press.

ADDITIONAL LEARNING RESOURCES

https://nptel.ac.in/courses/108102045/17
https://nptel.ac.in/courses/117106111/36
https://nptel.ac.in/courses/117104072/26
https://nptel.ac.in/courses/108107029/65

M. Tech. – II Semester
(19MT25707) NETWORK-ON-CHIP DESIGN
(Program Elective – 4)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on VLSI Design and parallel processing and Computing at UG Level

COURSE DESCRIPTION:

NOC –Architecture Design, Switching Technique ;Routing Algorithm ;Fault tolerance; Testing;3D NOC ;Optical NOC.

COURSE OBJECTIVES:

CEO1: To impart in-depth knowledge in Network on – chip Architecture and fault tolerance.
CEO2: To develop skills in design, analysis, problem solving and research in various routing algorithms.
CEO3: To apply knowledge and skills for development of applications in 3D Network On-chip Design.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand Network on-chip topologies, routing strategies and architectures to improve Quality of Service in communication applications.
CO2. Develop routing algorithms to solve problems of congestion and flow in multicast routing for 2D and 3D Mesh Networks.
CO3. Apply Security and Monitoring Services to reduce the occurrence of dead and Live lock condition during data transmission and Fault tolerance.
CO4. Analyze three-Dimensional Integration of Network-On-Chip for the development of Optical and 3D Network-On-Chip Architectures.

DETAILED SYLLABUS:

Unit – I: Introduction to NoC (Hours: 10)
Introduction to NoC, OSI layer rules in NoC, Interconnection Networks in Network-on-Chip Network Topologies, Switching Techniques, Routing Strategies, Flow Control Protocol Quality-of-Service Support-Optical NOC.

Unit – II: Architecture Design (Hours: 09)
Switching Techniques and Packet Format, Asynchronous FIFO Design, GALS Style of Communication, Wormhole Router Architecture Design, VC Router Architecture Design, Adaptive Router Architecture Design.

Unit – III: Routing Algorithm (Hours: 10)
Packet routing-QoS, congestion control and flow control, router design, network link design, Efficient and Deadlock-Free Tree-Based Multicast Routing Methods, Path-Based Multicast Routing for 2D and 3D Mesh Networks, Fault-Tolerant Routing Algorithms, Reliable and Adaptive Routing Algorithms.

Unit – IV: Test and Fault Tolerance Of NOC (Hours: 08)

Design-Security in Networks-on-Chips, Formal Verification of Communications in Networks, on-Chips Test and Fault Tolerance for Networks-on-Chip Infrastructures, Monitoring Services for Networks-on Chips.

Unit – V: Three-Dimensional Integration of Network-On-Chip (Hours: 08)

Three-Dimensional Networks-on-Chips Architectures, A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures, Resource Allocation for QoS On-Chip Communication, Networks-on-Chip Protocols-On-Chip Processor Traffic Modeling for Networks-on Chip.

Total Hours: 45

TEXT BOOK:

1. Chrysostomos Nicopoulos, Vijay krishnan Narayanan, Chita R.Das, "*Networks-on – Chip Architectures Holistic Design Exploration*", Springer.1st Edition, 2010.

REFERENCE BOOKS:

1. Fayezge bali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi *"Networks-on-Chips theory and practice",* 1ST Edition,2017CRC press.
2. Konstantinos Tatas and Kostas Siozios "*Designing 2D and 3D Network-on-Chip Architectures"* 1ST Edition,2014.
3. Palesi, Maurizio, Daneshtalab, Masoud "*Routing Algorithms in Networks-on-Chip"* 1ST Edition ,2014.
4. Santanu Kundu, Santanu Chattopadhyay "*Network-on-Chip: The Next Generation of System on-Chip Integration*", 1ST Edition,2017 CRC Press.

ADDITIONAL LEARNING RESOURCES

1. https://www.hindawi.com/journals/jece/2012/509465/
2. https://nptel.ac.in/courses/106103183/22

M. Tech. – II Semester
(19MT25708) RF IC Design
(Program Elective - 4)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Analog IC Design at UG Level/ PG Level.

COURSE DESCRIPTION:

Basics of RF IC Design, Assessment Parameters, Transceiver Architectures, Low Noise Amplifiers, Mixers, Oscillators, Phase Locked Loop, Power Amplifiers.

COURSE OBJECTIVES:

CEO1: To impart in-depth knowledge in developing transceivers as ICs operating at Radio Frequencies.
CEO2: To develop skills in design, analysis, problem solving and research in RFIC Design.
CEO3: To apply knowledge and skills for development of applications in RF systems.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Understand the various parameters used as metrics in the evaluation of RF IC designs.
CO2. Analyze the effects of Nonlinearity and transceiver architectures for the development of RF circuits.
CO3. Design Low Noise Amplifiers ,mixers, oscillators, Phase Locked loops and Power Amplifiers to operate efficiently at wide range of RF frequencies.

DETAILED SYLLABUS:

Unit – I: Basic Concepts in RF IC Design (Hours: 07)
Introduction to RF Design, Units in RF design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

Unit – II: Transceiver Architectures (Hours: 11)
General considerations, Receiver Architectures - Basic Heterodyne receivers, Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers, Low-IF receivers. Transmitter Architectures - Direct Conversion transmitters, Modern direct conversion Transmitters, Heterodyne Transmitters.

Unit – III: LNA and Mixers (Hours: 10)
General considerations, Problem of input matching, Low Noise Amplifiers design topologies, Gain Switching, Band Switching, Mixers - General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversion mixers.

Unit – IV: Oscillators (Hours : 08)
Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, phase noise, Quadrature Oscillators.

Unit – V: PLL and Power Amplifiers **(Hours: 09)**

PLLs - Phase detector, Type-I PLLs, Type-II PLLs, PFD/CP Non idealities, Phase noise in PLLs. Power Amplifiers - General considerations, Classification of power amplifiers, High - Efficiency power amplifiers, Linearization techniques.

Total Hours: *45*

TEXT BOOK:

1. B. Razavi, "*RF Microelectronics*", Prentice-Hall PTR, 2nd Edition, 1998.

REFERENCE BOOKS:

1. T.H.Lee, "*The Design of CMOS Radio-Frequency Integrated Circuits*", Cambridge University Press, 2nd Edition, 1998.
2. R.Jacob Baker, Harry W.Li, D.E. Boyce, "*CMOS Circuit Design, Layout and Simulation",* Prentice-Hall of India, 1998.

ADDITIONAL LEARNING RESOURCES:

http://www.mhhe.com/engcs/electrical/razavi/ppt.mhtml

https://nptel.ac.in/courses/117102012/

M. Tech. – II Semester
(19MT25731) PHYSICAL DESIGN AUTOMATION LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

A Course on VLSI Design at UG Level.

COURSE DESCRIPTION:

Graph Algorithms, Partitioning Algorithms, Floorplanning Algorithms, Routing Algorithms.

COURSE OBJECTIVES:

CEO1: To impart knowledge on modeling Design automation algorithms.
CEO2: To develop programming skills to solve problems in designing algorithms for Optimizing Physical Designs.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Demonstrate hands-on experience on modeling design automation algorithms by using the related EDA Tools.
CO2. Design and develop algorithms for optimizing physical designs.
CO3. Work individually and in groups to solve problems with effective communication.

List of Exercises/Experiments: (10-12 Exercises/Experiments)

1. Model the pseudo code for Depth First graph search algorithms for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

2. Model the pseudo code for Breadth First graph search algorithms for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

3. Model the pseudo code for spanning tree algorithm (Kruskal's Algorithm) for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

4. Model the pseudo code for shortest path algorithm (Dijkstra Algorithm) for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

5. Model the pseudo code for Steiner tree algorithm for optimization of designs using EDA Tool and assess the parameters like cut-set gain, number of nodes, branches, etc.

6. Model the pseudo code for Kernighan-Lin Partitioning algorithm for optimization of designs using EDA Tool and assess the parameters like cut-size, gain, area, etc.

7. Model the pseudo code for Simulated Annealing Partitioning algorithm for optimization of designs using EDA Tool and assess the parameters like cut-size, gain, area, etc.

8. Model the pseudo code for Constraint based Floorplanning algorithm for optimization of designs using EDA Tool and assess the parameters like area, contingency, etc.

9. Model the pseudo code for Integer Programming based Floorplanning algorithm for optimization of designs using EDA Tool and assess the parameters like area, contingency, etc.

10. Model the pseudo code for two terminal routing algorithm for optimization of designs using EDA Tool and assess the parameters like area, delay, etc.

11. Model the pseudo code for Lee's Maze routing algorithm for optimization of designs using EDA Tool and assess the parameters like area, delay, etc.

12. Model the pseudo code for Line Probe routing algorithm for optimization of designs using EDA Tool and assess the parameters like area, delay, etc.

13. Mini Projects (MPs):
    Form a group of maximum 2 members as a team and assign mini projects related to Development of algorithms for compaction of layouts.

REFERENCE BOOKS/LABORATORY MANUALS

1. ECE Department Physical Design Automation Lab Manual.
2. Naveed Shervani, *"Algorithms for Physical Design Automation"*, 3rd Edition, Kluwer Academic, 1998.
3. Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, *"Handbook of Algorithms for Physical Design Automation"*, CRC Press,2008.

SOFTWARE/Tools used:

Cadence/synopsys/mentor graphics

ADDITIONAL LEARNING RESOURCES

1. https://nptel.ac.in/noc/individual_course.php?id=noc17-cs15

M. Tech. – II Semester
(19MT25732) NANO MATERIALS AND NANOTECHNOLOGY LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

A Course on Circuit Level Design at UG Level.

COURSE DESCRIPTION:

Demonstration of Clean Room and Bench, Substrate Cleaning, Device Fabrication and Characterization, Verification of Device Characteristics in MATLAB and COMSOL, Visualization and Analysis of Carbon Allotropes.

COURSE OBJECTIVES:

CEO1: To impart knowledge on Design and Characterization of Nanoelectronic Devices.
CEO2: To design, fabricate and characterize Nanoelectronic devices.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Demonstrate hands-on experience on Clean Room, Substrate Preparation, Device fabrication and Characterization.
CO2. Design and develop nano devices for different applications in fields like electronics, biomedical, agriculture, etc.
CO3. Develop alternative nanostructures for the design of interdisciplinary applications.
CO4. Work individually and in groups to solve problems with effective communication.

List of Exercises/Experiments: (10-12 Exercises/Experiments)

Demonstration, fabrication and characterization of nano devices (8 Slots)

1. Demonstration of Clean room.
2. Demonstration of Clean bench.
3. Demonstration of substrate.
4. Cleaning process of substrate.
5. Fabrication of MOS using hydrothermal technique.
6. Deposition of filter by sol-gel method.
7. Deposition of thermal evaporation.
8. Device fabrication.
9. Device characterization for assessing the performance of the fabricated device.

Simulation and characterization of nano devices (4 Slots)

10. Verification of device characteristics by using MATLAB.
11. Verification of device characteristics by using COMSOL.
12. Visualization and analysis of carbon allotropes used in nanotechnology.

Total Time Slots: 12

REFERENCE BOOKS/LABORATORY MANUALS:

1. ECE Department Nano Materials and Nanotechnology Lab Manual.

Software/Tools used:

COMSOL and MATLAB

Hardware Equipment Required:

Clean Room, Spin Coater, chemicals, etc.

ADDITIONAL LEARNING RESOURCES

1. https://www.understandingnano.com/nanotechnology-research.html
2. http://www.nanoyou.eu/virtual-lab.html

M. Tech. – II Semester
(19MT2AC01) STATISTICS WITH R
(Audit Course)

(Common to All M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	2	-	-	-

PRE-REQUISITES: A course on Statistics.

COURSE DESCRIPTION:

Concepts of R programming basics, Bivariate and multivariate data, Confidence intervals, Goodness of fit, Analysis of variance.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1. Import, manage, manipulate, and structure data files using R programming.
CO2. Implement models for statistical analysis of a given dataset and visualize the results to identify trends, patterns and outliers in data.

DETAILED SYLLABUS:

UNIT I - INTRODUCTION **(Hours : 05)**

Data, R's command line, Variables, Functions, The workspace, External packages, Data sets, Data vectors, Functions, Numeric summaries, Categorical data.

Unit II - BIVARIATE AND MULTIVARIATE DATA **(Hours : 07)**

Lists, Data frames, Paired data, Correlation, Trends, Transformations, Bivariate categorical data, Measures of association, Two-way tables, Marginal distributions, Conditional distributions, Graphical summaries, Multivariate data - Data frames, Applying a function over a collection, Using external data, Lattice graphics, Grouping, Statistical transformations.

UNIT III - POPULATIONS **(Hours : 06)**

Populations, Discrete random variables, Random values generation, Sampling, Families of distributions, Central limit theorem, Statistical Inference - Significance tests, Estimation, Confidence intervals, Bayesian analysis.

UNIT IV - CONFIDENCE INTERVALS **(Hours : 06)**

Confidence intervals for a population proportion, *p* - population mean, Other confidence intervals, Confidence intervals for differences, Confidence intervals for the median, Significance test - Significance test for a population proportion, Significance test for the mean (t-tests), Significance tests and confidence intervals, Significance tests for the median.

UNIT V - GOODNESS OF FIT **(Hours : 06)**

The chi-squared goodness-of-fit test, The multinomial distribution, Pearson's χ^2-statistic, chi-squared test of independence and homogeneity, Goodness-of-fit tests for continuous distributions, ANOVA - One-way ANOVA, Using *lm* for ANOVA.

Total Hours: 30

TEXT BOOKS:

1. John Verzani, *Using R for Introductory Statistics*, CRC Press, 2nd Edition, 2014.
2. Sudha G Purohit, Sharad D Gore, Shailaja R Deshmukh, *Statistics Using R*, Narosa Publishing house, 2nd Edition, 2015.

REFERENCE BOOKS:

1. Francisco Juretig, *R Statistics Cookbook*, Packt Publishing, 1st Edition, 2019.
2. Prabhanjan N. Tattar, Suresh Ramaiah, B. G. Manjunath, *A Course in Statistics with R*, Wiley, 2018.

M. Tech. - III Semester
(19MT35731) INTERNSHIP

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	100	100	-	-	-	2

PRE-REQUISITES: --

COURSE DESCRIPTION: Expose students to the industrial environment; Create competent professionals for the industry; sharpen the real time technical / managerial skills required at the job; Gain professional experience and understand engineer's responsibilities and ethics.

COURSE OUTCOMES:

On successful completion of the course, students will be able to

CO1. Develop problem solving skills, critical thinking skills though designing and developing solutions for complex problems.
CO2. Utilize appropriate modern tools and techniques for implementing the proposed solutions.
CO3. Discern various challenges in developing solutions for complex problems, design and conduct experiments to evaluate alternative solutions for the chosen engineering problems.
CO4. Function effectively as an individual and participate well as a team member to build professional network for growth in career.
CO5. Develop communication, enrich professional, interpersonal and technical skills pertaining to the internship experience.
CO6. Utilize real work experiences to explore their interests, career alternatives that will help with future education or employment through and develop professional skills and competencies to engage in lifelong learning.

M. Tech. - III Semester
(19MT35732) PROJECT WORK PHASE-I

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	20	10

PRE-REQUISITES: --

COURSE DESCRIPTION:

Identification of topic for the project work; Literature survey; Collection of preliminary data; Identification of implementation tools and methodologies; Performing critical study and analysis of the problem identified; submitting a Report.

COURSE OUTCOMES:

On successful completion of the course, students will be able to

CO1. Apply contextual knowledge to identify specific domain in VLSI and allied areas of discipline.
CO2. Conduct literature review, analyze, cognize and comprehend the extracted information to recognize the current status of research pertinent to the chosen domain.
CO3. Select appropriate tools, techniques and resources for implementation of project work.
CO4. Function effectively as an individual to recognize the opportunities in the chosen domain of interest
CO5. Write and present a technical report/document to present the findings on the chosen problem.
CO6. Engage lifelong learning for development of technical competence in the field of VLSI.

M. Tech. - IV Semester
(19MT45731) PROJECT WORK PHASE-II

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
150	150	300	-	-	32	16

PRE-REQUISITES: --

COURSE DESCRIPTION:

Time and cost analysis; undertaking practical investigations of project work; implementation; analysis of results; validation and report writing.

COURSE OUTCOMES:

On successful completion of the course, students will be able to

CO1. Design and develop Integrated Circuits/systems/platforms to undertake practical investigations of project work, analyze and interpret results.
CO2. Utilize appropriate tools, techniques and resources for implementation of project work.
CO3. Function effectively as an individual to recognize the opportunities in the chosen domain of interest
CO4. Write and present a technical report/document to present the findings on the chosen problem.
CO5. Engage lifelong learning for development of technical competence in the field of VLSI.