SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, Near Tirupati – 517102

Department of Electronics and Communication Engineering

Report on One week AICTE Sponsored Short Term Training Programme on *Recent Trends and Research Challenges on Nano CMOS VLSI Circuits by Industry Standard EDA Tools* (26- 31 August, 2019)

Research and development in VLSI system have been growing in the public and private sectors in both developed and developing countries. The continuous increase of integration densities in CMOS technology has driven the rapid growth of VLSI circuit for today's high-tech electronics industries from consumer products to telecommunications and computers. As CMOS technologies are scaled down into the nanometer range IC design and testing have become a real challenge to ensure the functionality and quality of the product.

In the glow of these developments, Sree Vidyanikethan Engineering College, Tirupati has organized All India Council of Technical Education (AICTE) Sponsored Short Term Training Programme (STTP) on "**Recent Trends and Research Challenges on NANO CMOS VLSI circuits by Industry Standard EDA Tools"** as a forum on new and emerging applications in handheld and portable devices.

The intention of the Short Term Training Programme is to make the faculty and Research scholars understanding the analysis of Nano CMOS logic design process and optimization techniques, also equipped to capture the research challenges posed by Nano CMOS chip design industry

The STTP on Nano CMOS VLSI design and Industry Standard Tools proved their efficiency to

- Design and analyze entire semiconductor chip
- Modern semiconductor chip can have billions of components so EDA tools are essential for their design
- Enhance the designing and programming skills in Nano CMOS VLSI
- Deliver the research contribution towards the societal needs
- Reduce the device dimension by applying different Nano materials in CMOS design
- Explore fundamentals of new device structure and new material availability in the technology transformation.

This STTP is to bring together leading scientists, Industrialists, Key Stakeholders and Experts, in order to promote the presentation of research , industry results and the discussion of experiences.

Objective of Short Term Training Programme

The Short Term Training Programme has been considered to envelop the following objectives

- To upgrade the knowledge of academicians and practioners who are involved in teaching /research/industry in the field of Nano CMOS VLSI circuits.
- To strengthen the VLSI activities among the faculty and researchers by giving hands on experience on the usage of various industrial standard EDA tools.
- To emphasize the pedagogy of learning by analyze and apply the experience on the various methodologies and techniques in Nano VLSI domain.
- To Orient the teaching and research community to solve the critical research issues in the Nano CMOS domain
- To provide forum to exchange views, ideas and innovations with eminent experts in the field of Nano CMOS VLSI design.
- To helps to identify the thrust areas and developing new applications and enhance the curriculum development of quality teaching.

DAY 1 (26.08.2019)

Inauguration

The Programme was inaugurated by Mr. Nagendra Bandi, Sr. Application Engineer, CoreEL Technologies, Bangalore, Dr. D. V. S. Bhagavanulu, Director SVEC, Dr. I. Sudharsan Kumar, Director (Q & D), SVET, Dr. P. V. Ramana, Professor & Head, Department of ECE, SVEC and Dr. N. Vithyalakshmi, Associate Professor, Department of ECE, SVEC.

Lighting the Lamp by Dr. D. V. S. Bhagavanulu, Director SVEC , Dr. P. V. Ramana, Professor & Head, Department of ECE

Welcome address by Co-ordinator Dr. N. Vithyalakshmi, Associate Professor, Department of ECE

Dr. P. V. Ramana, Professor & Head of ECE department addressing the participants

Chief Guest Mr. Nagendra Bandi, Sr. Application Engineer, CoreEL Technologies, Bangalore addressing the participants

		
Dr. I. Sudharsan Kumar, Director (Q & D), SVET addressing the participants		***Dr. D. V. S. Bhagavanulu, Director SVEC addressing the participants***

Session 1: Full custom design flow- Schematic entry Using Mentor Graphics Tool

The speaker highlighted the importance of EDA solutions for VLSI design methodology and the capabilities of Mentor Graphics HEP2 tools as well learn the flow of the Full Custom IC design cycle. He explained very clearly how to create various components like inverter, NAND gate, XOR gate, Full adder, Latch, SRAM register cell and PLL, differential amplifier and running of DRC, LVS and Parasitic Extraction on the various designs. Finally he demonstrated how the circuit is verified by doing various simulations using ELDO. In the process, participants can learn to use EZviewer, waveform window options, waveform calculator, etc...

Mr.Nagendra Bandi, CoreEL Technologies, Bangalore explaining the EDA solution for VLSI design methodology

Session 2: Hands on Training using Mentor Graphics Tool

The session was provided to have hands on experience of schematic entry for full custom design using the technology library GDK 130nm (Generic13). The participants practiced to build the schematic of design by instantiating various components. Once the schematic is done then they learned how to generate the symbol for the particular design like basic gates and universal gates, SRAM register cell and PLL, differential amplifier.

Creating a Schematic:

In this section participants can familiar with placing primitive analog and digital devices for any design also can learn how to

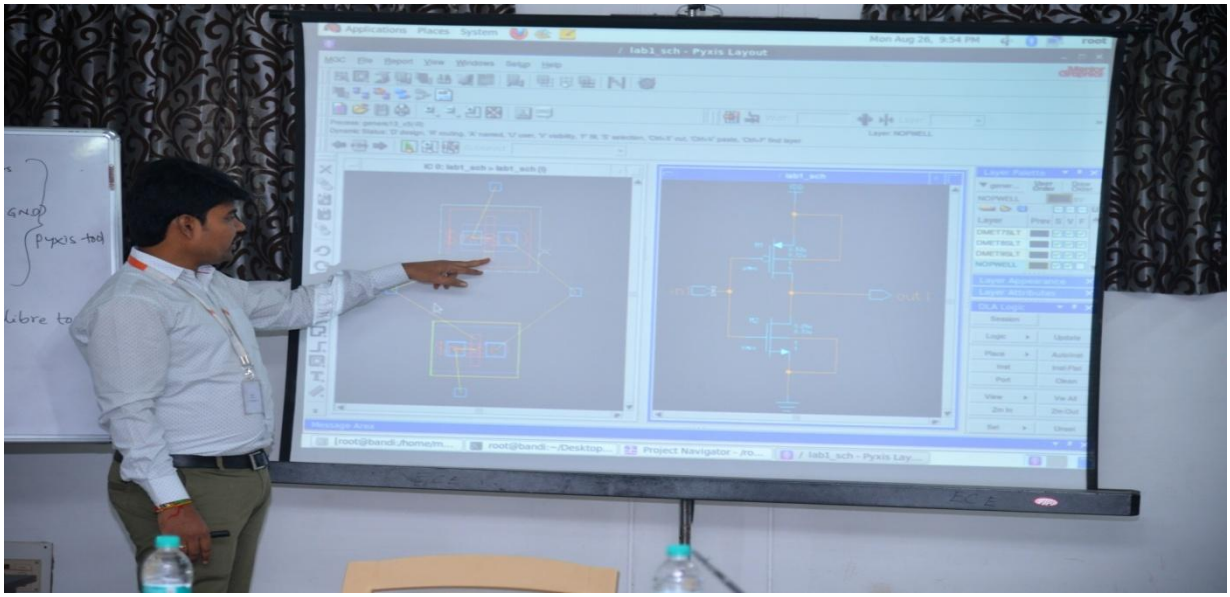
- Place primitives on the schematic
- Select and manipulate devices
- Customizing hotkeys for placing devices
- Route devices
- Edit device parameter values
- Name instances
- Check and save the schematic
- Create upper hierarchical symbols
- Create test bench
- Simulate using Eldo
- View results

Participants clarifying their doubts with Resource person

DAY 2 (27.08.2019)

Session 3: Layout entry using Mentor Graphics Tool

The Resource person demonstrated the Pyxis Layout Editor basics by concentrating on designing an "Inverter" through automatic layout generation. Then he explained to completing the other layouts, generating GDSII file. After that, by taking GDSII file as reference he taught us to run DRC, LVS checks on the layout, Extract parasitic and back-annotate them to the simulation environment.



Mr.Nagendra Bandi, CoreEL Technologies, Bangalore explaining Layout Editor Basics with example

Session 4: Hands on Training using Mentor Graphics Tool

The participants had hands on experience of layout based entry for full custom design using Pyxis and Calibre Tool. The participants practiced for basic gates and universal gates using layer information.

Procedure to draw the Layout for the circuit using Pyxis Layout.

- Create new Layout window
- Create and setup SDL window
- Add the layout of Transistors
- Select the Iroute and interconnect Tools
- Connect the I/O ports , VDD, Ground
- Run the physical verification (DRC, LVS, PEX) using Calibre tool.
- Run the post layout simulation by adding the .dspf file generated in PEX.
- Observe the post layout results

DAY 3 (28.08.2019)

Session 5: Semicustom design flow on 7 series FPGA (ZYNQ 7000-Zed Board)

The session started with introduction advanced FPGAs and their capabilities. The Vivado Tool was introduced and counter was designed using Zed board of Zynq -7000 family. Participants can also use Mark Debug feature and also the available Integrated Logic Analyzer (ILA) core (in IP Catalog) to debug the hardware.

Mr. Nagendra Bandi, CoreEL Technologies, Bangalore demonstrating advanced FPGA and Vivado Tool

Session 6: Hands on Training using Vivado Tool

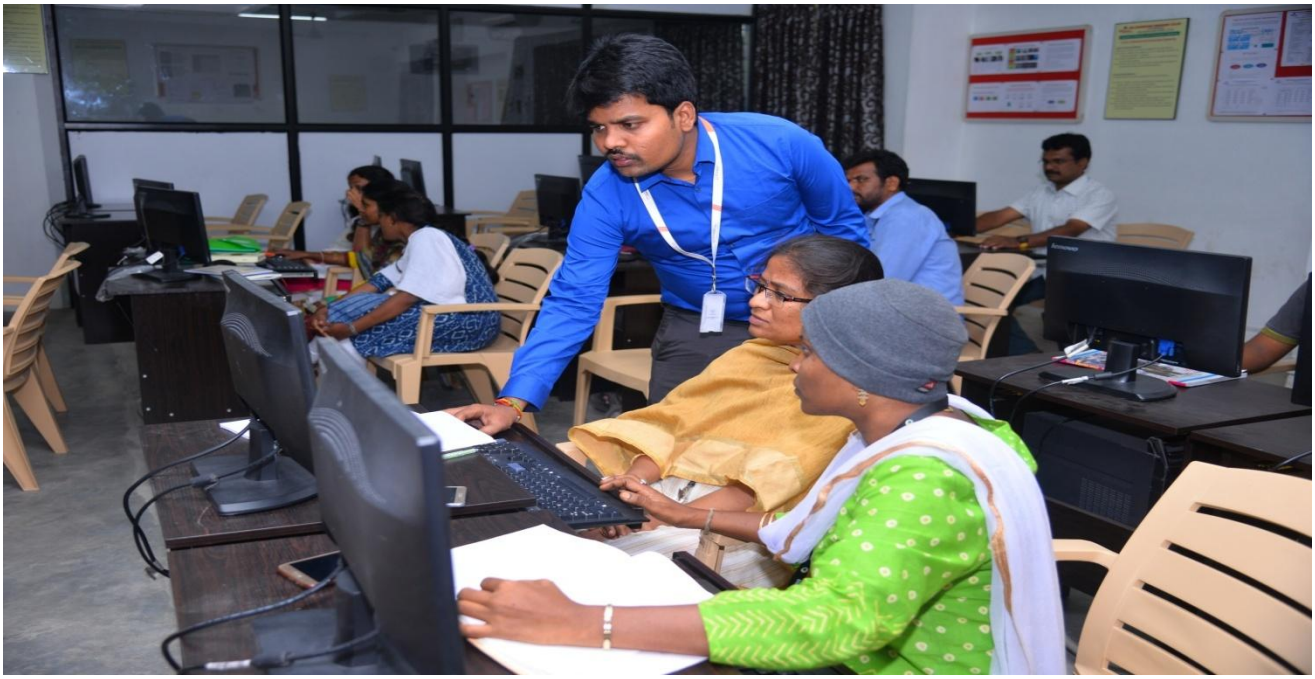
The participants had familiarity in the process of using Vivado IDE to create a simple HDL design targeting the ZedBoard. Also able to simulate, synthesize, and implement the design with default settings. Finally, users can generate the bitstream and download it in to the hardware to verify the design functionality by using ILA (Integrated logic Analyzer, virtual Input output, etc.,) by interfacing Zed board with Vivado Tool.

General Flow of Tool

Step 1: Create a Vivado Project using IDE
Step 2: Simulate the Design using Vivado Simulator
Step 3: Synthesize the Design and Mark Debug
Step 4: Implement and Generate Bitstream
Step 5: Perform the Timing Simulation
Step 6: Verify Functionality in Hardware

After completing this Tool, participants can be able to:

- Create a Vivado project sourcing HDL model(s) and targeting a specific FPGA device located on the ZedBoard
- Use the provided Xilinx Design Constraint (XDC) file to constrain the pin locations
- Simulate the design using the Vivado simulator
- Synthesize and implement the design
- Generate the bitstream
- Configure the FPGA using the generated bitstream and verify the functionality



Resource person supporting the participants to debug errors

DAY 4 (29.08.2019)

Session 7: Schematic design entry for 2D CMOS using TCAD Tool

The Resource person introduced Visual TCAD Tool and various Nano meter scales in which the tools support. Also the trainer demonstrated how to use the tool for Device Modeling, Simulation and Characterization of the Device (transistors and diodes) are done using different methods. Analytical method is used for modeling which consists of closed form equations obtained using spice. Experimental method is required for characterization. Numerical methods which are based on the concept of 2D/3D meshing can be adopted for conducting simulation studies which requires Technology CAD.

Mr.Nitish Kumar , Cadre design systems, Ghaziabad demonstrating Visual TCAD Tool to the participants

Session 8: Hands on Training using TCAD Tool

The participants developed PN diode, PMOS, NMOS and CMOS devices also visualized various characteristics of the device like band gap diagram, potential variation, electron and hole density etc., by using TCAD Tool

Various steps followed for device simulation are

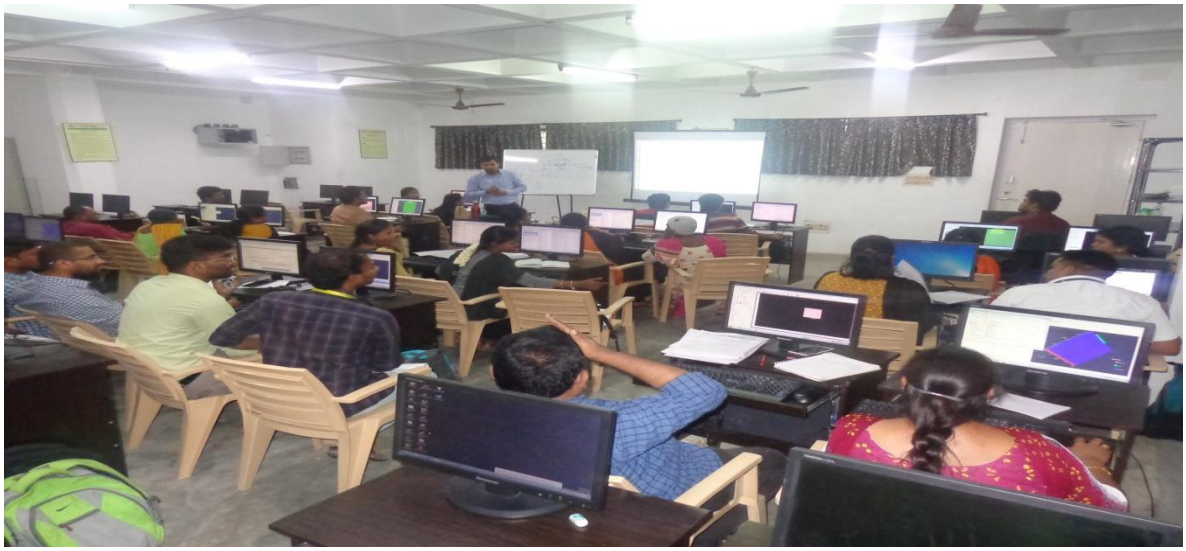
- Define X,Y, and Z mesh
- Define regions and corresponding materials
- Define doping Profile
- Apply models
- Apply bias
- Export the output file

Resource person giving hands on Training to the Participants

DAY 5 (30.08.2019)

Session 9: Layout entry using TCAD K-Layout Tool

The resource person introduced K-Layout Tool editor and explained the various option that are useful to develop layout at Nano scale. He demonstrated the design of NMOS Layout



Mr. Nitish Kumar , Cadre design systems, Ghaziabad explaining K-Layout Tool to the participants

Session 10: Hands on Training using K-Layout Tool

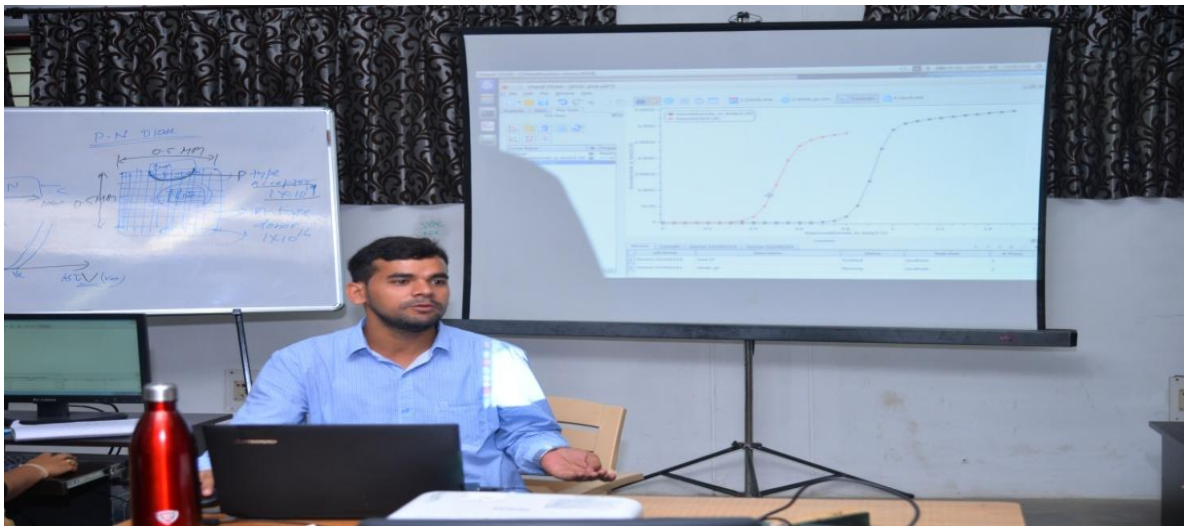
The participants experienced PMOS, NMOS and CMOS devices using K-Layout Tool and visualized the 3D structure for developed devices

Participants are practicing the Tool with example

DAY 6 (31.08.2019)

Session 11: Schematic design entry for 3D CMOS, FinFET and CNTFET Using TCAD Tool

The trainer specified alternative ways of developing devices using TCAD Tool. (i.e) By using schematic, Layout and scripting language based coding. The design of FinFET and CNTFET was demonstrated at 20nm Technology.



Mr.Nitish Kumar, Cadre design systems, Ghaziabad explaining the 3D models of FinFET

Session 12: Hands on Training using TCAD Tool

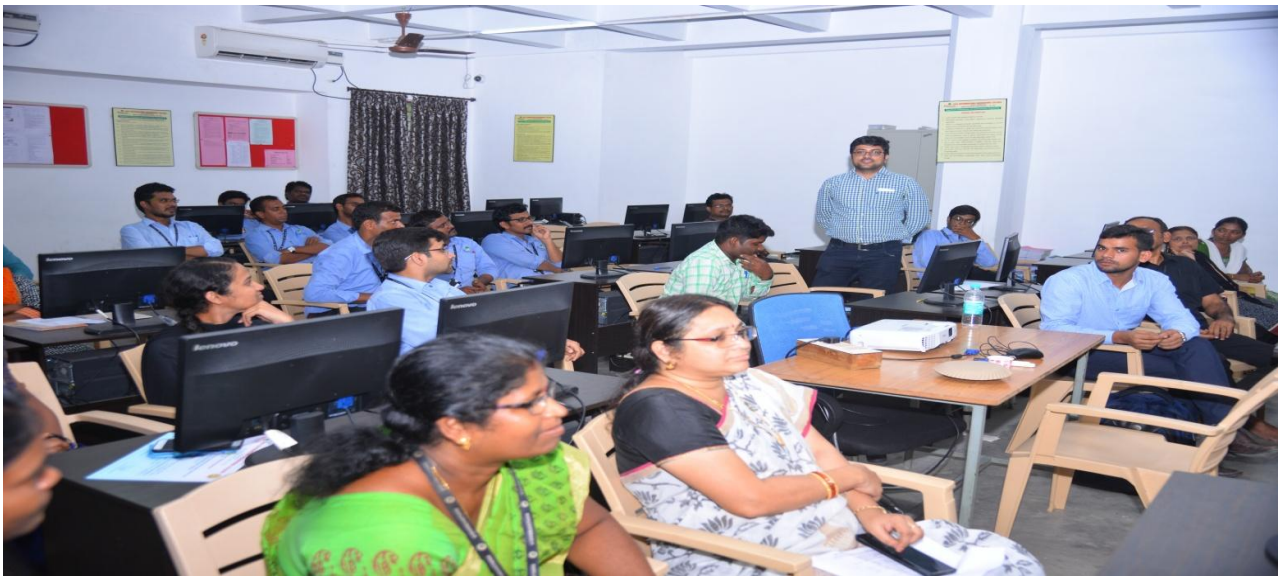
The participants proficient in Trigate FET and CNTFET designs and the corresponding circuit development using TCAD and K-Layout Tools.

Participants practicing the Tool

Valedictory Function

The Valedictory function was held on 31-08-2019 at 4.00 PM with Chief guest and Guests of honour Mr. Nitish Kumar Application Engineer, Cadre design systems, Ghaziabad, Dr. P. V. Ramana, Professor & Head, Department of ECE, SVEC, Dr. V. R. Anitha, Professor, Department of ECE, Dr. N. Padmaja, Professor, Department of ECE and Dr. N. Vithyalakshmi, Associate Professor, Department of ECE, SVEC and certificates were distributed to the participants, finally the programme was concluded by vote of thanks

Certificate distributed to participant by Mr.Nitish Kumar, Cadre design systems, Ghaziabad.



Feedback given by External Participant about one week AICTE sponsored Short Term Training Programme