ACADEMIC REGULATIONS

COURSE STRUCTURE

AND

DETAILED SYLLABI

For

MASTER OF TECHNOLOGY

In

Digital Electronics and Communication Systems (DECS)

(For the batches admitted from 2019-2020)

CHOICE BASED CREDIT SYSTEM

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)

(Affiliated to JNTU Anantapur, Approved by AICTE
Programs Accredited by NBA; NAAC with 'A' grade)
Sree Sainath Nagar, A.Rangampet, Near Tirupati - 517 102.A.P.

VISION

To be one of the Nation's premier Engineering Colleges by achieving the highest order of excellence in Teaching and Research.

MISSION

- To foster intellectual curiosity, pursuit and dissemination of knowledge.
- To explore students' potential through academic freedom and integrity.
- To promote technical mastery and nurture skilled professionals to face competition in ever increasing complex world.

QUALITY POLICY

Sree Vidyanikethan Engineering College strives to establish a system of Quality Assurance to continuously address, monitor and evaluate the quality of education offered to students, thus promoting effective teaching processes for the benefit of students and making the College a Centre of Excellence for Engineering and Technological studies.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To be a center of excellence in Electronics and Communication Engineering through teaching and research producing high quality engineering professionals with values and ethics to meet local and global demands.

MISSION

- The Department of Electronics and Communication Engineering is established with the cause of creating competent professionals to work in multicultural and multidisciplinary environments.
- Imparting knowledge through contemporary curriculum and striving for development of students with diverse background.
- Inspiring students and faculty members for innovative research through constant interaction with research organizations and industry to meet societal needs.
- Developing skills for enhancing employability of students through comprehensive training process.
- Imbibing ethics and values in students for effective engineering practice.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M. Tech. (Digital Electronics and Communication Systems)

PROGRAM EDUCATIONAL OBJECTIVES

After few years of graduation, the graduates of M. Tech. (DECS) Program would have

PEO1. Enrolled or completed research studies in the core or allied areas of Digital Electronics and Communication Systems.

PEO2. Successful entrepreneurial or technical career in the core or allied areas of Digital Electronics and Communication Systems.

PEO3. Continued to learn and to adapt to the world of constantly evolving technologies in the core or allied areas of digital electronics and communication systems.

PROGRAM OUTCOMES

On successful completion of the Program, the graduates of M. Tech. (DECS) will be able to:

PO1. Demonstrate mastery of knowledge in Digital Electronics, Communication Systems and other allied areas of the program.

PO2. Design and develop Electronic and Communication systems for communication and signal processing applications.

PO3. Select and apply appropriate modern tools, techniques and resources to provide engineering solutions in Digital Electronics, Communication Systems and allied areas.

PO4. Independently carry out research to deliver solutions for complex problems in Digital Electronics and Communication Systems.

PO5. Communicate effectively in written and oral formats.

PO6. Ability to continuously engage in life-long learning to enhance knowledge and competence.

The Challenge of Change

"Mastery of change is in fact the challenge of moving human attention from an old state to a new state. Leaders can shift attention at the right time and to the right place. The real crisis of our times is the crisis of attention. Those who lead are the ones who can hold your attention and move it in a purposeful way. Transformation is nothing but a shift in attention from one form to another. The form of a beautiful butterfly breaks free from a crawling caterpillar. If you pay enough attention, you would be able to see how the butterfly hides within the caterpillar. The leader points out a butterfly when the follower sees only a caterpillar".

- Debashis Chatterjee

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(AUTONOMOUS)

(Affiliated to J.N.T. University Anantapur, Ananthapuramu)

ACADEMIC REGULATIONS
(SVEC-19)

CHOICE BASED CREDIT SYSTEM

M. Tech. Regular Two Year Degree Program

(For the batches admitted from the academic year 2019-2020)

For pursuing Two year degree program of study in Master of Technology (M.Tech) offered by Sree Vidyanikethan Engineering College under Autonomous status and herein after referred to as SVEC:

1. Applicability: All the rules specified herein, approved by the Academic Council, shall be in force and applicable to students admitted from the academic year 2019-2020 onwards. Any reference to "College" in these rules and regulations stands for SVEC.

2. Extent: All the rules and regulations, specified hereinafter shall be read as a whole for the purpose of interpretation and as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. It shall be ratified by Academic Council in the forth coming meeting. As per the requirements of statutory bodies, Principal, SVEC shall be the Chairman, Academic Council.

3. Admission :

3.1. Admission into the Two Year M. Tech. Degree Program:

3.1.1. Eligibility:

A candidate seeking admission into the two year M. Tech Degree Program should have

(i) Passed B.Tech/B.E or equivalent Program recognized by JNTUA, Ananthapuramu, for admission as per the guidelines of Andhra Pradesh State Council of Higher Education (APSCHE).

(ii) A minimum percentage of marks in the qualifying degree as prescribed by the AICTE / UGC or Government at the time of admission.

(iii) Rank/score secured in the PGECET/GATE examination conducted by APSCHE/ MHRD for allotment of a seat by the convener PGECET, for admission.

3.1.2. Admission Procedure:

Admissions are made into the two year M.Tech. Degree Program as per the stipulations of APSCHE, Government of Andhra Pradesh:

(a) By the Convener, PGECET (for Category–A Seats)

(b) By the Management (for Category-B Seats).

4. Programs of study offered leading to the award of M.Tech. Degree and Eligibility:

Following are the two year M.Tech degree Programs of study with specializations, offered by the departments in SVEC leading to the award of M.Tech. degree and the qualifying degree eligible for admission:

<table>
<tr><th>Name of the M.Tech specialization</th><th>Offered by the Department</th><th>Qualifying Degree / Branch eligible for Admission</th></tr>
<tr><td>Electrical Power Systems</td><td rowspan="2">EEE</td><td rowspan="2">BE/ B.Tech / AMIE in Electrical & Electronics Engineering / Electrical Engineering or equivalent</td></tr>
<tr><td>Power Electronics and Drives</td></tr>
<tr><td>Digital Electronics and Communication Systems</td><td rowspan="3">ECE</td><td rowspan="2">BE / B.Tech in ECE / AMIE in ECE, AMIE (Electronics & Telecommunication Engineering) / AMIETE (Electronics & Telematics Engineering)/ Electronics & Computer Engineering/ Electronics/ Electronics & Telematics or equivalent</td></tr>
<tr><td>Communication Systems</td></tr>
<tr><td>VLSI</td><td>BE / B.Tech / AMIE in ECE, / EEE / CSE / Electronics & Computer Engineering / ETE / IT / CSIT / Electronics and Control Engineering / Instrumentation Engineering / Instrumentation Technology / EIE / Electronics Engineering / Bio-Medical Engineering / AMIETE (Electronics & Telematics Engineering)/ Electronics or equivalent</td></tr>
<tr><td>Computer Science</td><td rowspan="2">CSE</td><td rowspan="3">BE / B.Tech / AMIE in CSE / CSIT / IT / CSSE ,
M.Sc. (Computer Science), M.Sc. (Information Systems), M. Sc. (Information Technology), MCA or equivalent.</td></tr>
<tr><td>Computer Networks and Information Security</td></tr>
<tr><td>Software Engineering</td><td>IT</td></tr>
</table>

5. Duration of the Program:

5.1 Minimum Duration:

The program will extend over a period of two years leading to award of the Degree of Master of Technology (M.Tech) by JNTUA University, Ananthapuramu. The two academic years are divided into four semesters with two semesters per year. Each semester shall consist of 21 weeks (≥90 working days) having – 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) as suggested by UGC, and Curriculum/Course Structure as suggested by AICTE are followed.

5.2 Maximum Duration:

The student shall complete all the passing requirements of the M.Tech degree program within a maximum duration of 04 years excluding the Gap year. This duration is reckoned from the commencement of the semester into which the student is first admitted to the program.

6. Course Structure:

Each M.Tech Program of study shall comprise of:

- Professional Core courses:

  The list of professional core courses shall be chosen as per the suggestions of the experts, to impart knowledge and skills needed in the concerned specialization of study.

- Professional Elective courses:

  Professional elective courses shall be offered to the students to diversify their spectrum of knowledge and skills. The elective courses can be chosen based on the interest of the student to broaden his individual knowledge and skills.

- Audit Courses: Audit courses shall be offered to the students to diversify their knowledge.

- Projects (Internship, Project work)

7. Credit System: All Courses are to be registered by a student in a Semester to earn Credits. Credits are assigned based on the following norms given in Table 1.

Table 1

Course	Periods/Week	Credits
Theory	01	01
Practical	01	0.5
Internship	--	02
Project Work Phase-I	--	10
Project Work Phase-II	--	16

All Courses are to be registered by a student in a Semester to earn Credits. Credits shall be assigned to each Course in an L: T: P: C (Lecture Hours: Tutorial Hours: Practical Hours: Credits) Structure, based on the following general pattern.

- **Theory Courses:** One Lecture Hour (L) per week in a semester: 01 Credit
- **Practical Courses:** One Practical Hour (P) Per week in a semester: 0.5 Credit
- **Tutorial:** One Tutorial Hour (T) Per week in a semester: 01 Credit
- **Audit Courses:** No **CREDIT** is awarded.
- **Open Elective** (MOOC): 03 Credits

For courses like Internship and Project work, where formal contact periods are not specified, credits are assigned based on the complexity of the work to be carried out. Other student activities like NCC, NSS, Sports, Study Tour, and Guest Lecture etc. shall not carry Credits.

The two year curriculum of any M. Tech Degree Program of study shall have total of **68** credits.

8. Choice Based Credit System (CBCS):

8.1 Choice Based Credit System (CBCS) is introduced in line with UGC guidelines in order to promote:

- Student centered learning
- Students to learn courses of their choice
- Interdisciplinary learning

A Student has a choice of registering for courses comprising program core, Program electives, Open elective through MOOC course.

9. Course Enrollment and Registration

9.1 Each student, on admission shall be assigned to a Faculty Advisor (Mentor) who shall advice and counsel the student about the details of the academic program and the choice of courses considering the student's academic background and career objectives.

9.2 The enrollment of courses in I-Semester will commence on the day of admission. If the student wishes, the student may drop or add courses (vide clause 8) within **three** days before commencement of I-Semester class work and complete the registration process. The student shall enroll for the courses with the help of Faculty Advisor (Mentor). The enrollment of courses in II-Semester will commence 10 days prior to the last instructional day of the I-Semester and complete the registration process for all the remaining theory courses as per program course structure, duly authorized by the Chairman, Board of studies of concerned department.

9.3 If any student fails to register the courses in a semester, he shall undergo the courses as per the program course structure.

9.4 After registering for a course, a student shall attend the classes, satisfy the attendance requirements, earn Continuous Assessment marks and appear for the Semester-end Examinations.

9.5 No elective course shall be offered by a Department unless a minimum of 08 students register for the course.

10. OPEN ELECTIVE (MOOC):

OPEN ELECTIVE (MOOC) is an online course aimed at unlimited participation and open access via the web.

10.1 A Student is offered an Open Elective (MOOC), in the M.Tech II-Semester, and pursued through Massive Open Online Course (MOOC) platforms.

10.2 The student shall confirm registration by enrolling the course within 10 days prior to the last instructional day of the M.Tech I-Semester along with other courses.

10.3 The list of courses along with MOOC service providers shall be identified by the Chairman, BOS, and Head of the Department. The identified Open Elective (MOOC) courses are to be approved by the Chairman, Academic Council.

10.4 The HOD shall appoint one faculty member as **mentor** during the M.Tech I-Semester for each Open Elective Course registered through MOOC.

10.5 There shall be ONLY semester-end examination for open elective (MOOC) course. It shall be evaluated by the department through ONLINE with 50 multiple choice questions for 100 marks. The department shall prepare the Question Bank for Conducting the ONLINE Open Elective (MOOC) Examination.

11. Break of Study from a Program (Gap Year)

11.1 A student is permitted to go on break of study for a maximum period of one year.

11.2 The student shall apply for break of study in advance, in any case, not later than the last date of the first assessment period in a semester. The gap year concept is introduced for start-up (or) incubation of an idea, National/International Internships, professional Volunteering and chronic illness.The application downloaded from the website and duly filled in by the student shall be submitted to the Principal through the Head of the department. A committee shall be appointed by the Principal in this regard. Based on the recommendations of the committee, Principal shall decide whether to permit the student to avail the gap year or not.

11.3 The students permitted to rejoin the program after break of study shall be governed by the Curriculum and Regulations in force at the time of rejoining.

The students rejoining in new regulations shall apply to the Principal in the prescribed format through Head of the Department, at the beginning of the readmitted semester for registering additional/equivalent courses to comply with the curriculum in-force.

11.4 The one year period of break of study shall not be counted for the maximum period for the award of the degree (i.e 05 years shall be the maximum period for the award of degree for the students availing Gap Year).

11.5 If a student has not reported to the college after completion of approved period of break of study without prior intimation, he is deemed to be detained in that semester. Such students are eligible for readmission into the semester when offered next.

12. Examination System: All components in any Program of study shall be evaluated through internal evaluation and/or an external evaluation conducted as semester-end examination.

12.1. Distribution of Marks:

Sl. No.	Course	Marks	Examination and Evaluation	Scheme of examination
1.	Theory	60	Semester-end examination of 3 hours duration (External evaluation)	The examination question paper in theory courses shall be for a maximum of 60 marks. The question paper shall be of descriptive type with 10 questions each of 12 marks, taken two from each unit. Each unit will have internal choice and 5 questions shall be answered, one from each unit.
		40	Mid-term Examination of 2 hours duration (Internal evaluation).	Two mid-term examinations each for 40 marks are to be conducted. For a total of 40 marks, 80% of better one of the two and 20% of the other one are added and finalized. **Mid-I:** After first spell of instruction (I & II Units). **Mid-II**: After second spell of instruction (III, IV & V Units). The question paper shall be of descriptive type with 5 essay type questions each of 10 marks, out of which 3 are to be answered and evaluated for 30 marks. There shall be also 5 short answer questions each of 2 marks, all are to be answered and evaluated for 10 marks.

Sl. No.	Course	Marks	Examination and Evaluation		Scheme of examination
2	Laboratory	50	Semester-end Lab Examination for 3 hours duration (External evaluation)		The examination will be conducted by the faculty member handling the laboratory (Examiner-2) and another faculty member (Examiner-1) appointed by the Chief Controller of examinations.
		50	30	Day-to-Day evaluation for Performance in laboratory experiments and Record. (Internal evaluation).	Two laboratory examinations, which include Day-to-Day evaluation and Practical test, each for 50 marks are to be evaluated by the faculty members handling the laboratory. For a total of 50 marks 80% of better one of the two and 20% of the other one are added and finalized. **Laboratory examination-I:** Shall be conducted just before FIRST mid-term examinations. **Laboratory examination-II:** Shall be conducted just before SECOND mid-term examinations.
			20	Practical test (Internal evaluation).	
3	Audit Courses	--	--		As detailed in 12.2.1
4	Internship	100	Semester-end Examination		100 marks are allotted for Internship During semester-end evaluation by the Department Evaluation Committee (**DEC**) as given in 12.2.2.
5	Open Elective (MOOC)	100	Semester-end Examination		The evaluation shall be done by the department through ONLINE with 50 multiple choice questions.
6	Project Work Phase-I	100	50	Internal evaluation	Continuous evaluation shall be done by the Project Evaluation Committee (**PEC)** as given in 12.2.3.1
			50	Semester-end evaluation	Project Work Viva-Voce Examination shall be conducted by a Committee at the end of the semester as given in 12.2.3.1
7	Project Work Phase-II	300	150	Internal evaluation	Continuous evaluation shall be done by the Project Evaluation Committee (**PEC)** as given in 12.2.3.2
			150	Semester-end evaluation	Project Work Viva-Voce Examination shall be conducted by a Committee at the end of the semester as given in 12.2.3.2

12.2 Audit Course/ Internship and Project Work Evaluation:

12.2.1. Audit Course:

Audit courses carry "ZERO" credits. There shall be **NO Internal Examination** and **Semester-end examination**. However, ATTENDANCE in Audit courses shall be considered while calculating aggregate attendance in a semester. The student should study all the audit courses, and it will be indicated in the GRADE Sheet.

12.2.2. Internship:

The student shall undergo **Internship** in an Industry/National Laboratories/Academic Institutions relevant to the respective branch of study. This course is to be registered during II-Semester and taken up during the summer vacation after completion of the II-Semester, for a period of FOUR weeks duration. The Industry training/Internship shall be submitted in a Report form, and a presentation of the same shall be made before a Department Evaluation Committee (DEC) and it should be evaluated for 100 marks. The DEC shall consist of the Head of the

Department, the concerned Supervisor and a Senior Faculty Member of the Department. The DEC is constituted by the Chief Controller of Examinations on the recommendations of the Head of the Department. There shall be NO internal marks for Internship. The Internship shall be evaluated at the end of the III-Semester.

12.2.3. Project Work:

12.2.3.1. The Project Evaluation Committee (PEC) consisting of concerned supervisor and two senior faculty members shall monitor the progress of the project work of the student. The PEC is constituted by the Principal on the recommendations of the Head of the Department. Project Work Phase–I is to be completed in the III-Semester. A Student has to identify the topic of the Project Work, collect relevant Literature, preliminary data, implementation tools/ methodologies etc., and perform a critical study and analysis of the problem identified and submit a Report.

(i) **Internal Evaluation:** The Internal Evaluation of Project work Phase-I shall be made by the PEC on the basis of TWO project reviews on the topic of the project. Each review shall be conducted for a maximum of "50" marks. For a total of 50 marks, 80% of better one of the two and 20% of the other one are added and finalized.

(ii) **Semester-end Evaluation:** The semester-end Project Work Phase-I Viva-Voce examination shall be conducted by the concerned guide and a senior faculty member recommended by the Head of the Department and appointed by the Chief Controller of Examinations.

12.2.3.2 A student shall continue to undertake the Project Work Phase–II during the IV Semester by undertaking practical investigations, implementation, analysis of results, validation and report writing. The student shall submit a Project report at the end of the semester after approval of the PEC.

(i) **Internal Evaluation:** The Internal Evaluation of Project work Phase-II shall be made by the PEC by conducting TWO project reviews on the progress, presentations and quality of work. Each review shall be conducted for a maximum of "150" marks. For a total of 150 marks, 80% of better one of the two and 20% of the other one are added and finalized.

(ii)**Semester-end Evaluation:** A candidate shall be allowed to submit the dissertation on the recommendations of the PEC. Three copies of the dissertation certified in the prescribed format by the concerned Supervisor and HOD shall be submitted to the Department. One copy is to be submitted to the Chief Controller of Examinations and one copy to be sent to the examiner. The examiner shall be nominated by the Chief Controller of the Examinations from the panel of THREE examiners submitted by the Department for a maximum of 05 students at a time for adjudication.

If the report of the examiner is favorable, Semester-end Project Work Phase-II Viva-Voce Examination shall be conducted by a Committee consisting of External examiner (nominated by the Chief Controller of Examinations), HOD and concerned Supervisor at the end of the IV Semester.

If the report of the examiner is not favorable, the dissertation should be revised and resubmitted after a minimum period of three months.

12.2.3.3 The students who fail in Project work Phase-I (or) Phase-II Viva-Voce examination shall have to re-appear for the Viva-Voce examination after three months. Extension of time for completing the project is to be obtained from the Chairman, Academic Council, SVEC (Autonomous).

12.2.3.4 Change of the project work topic shall be permitted only in Project Work Phase-I, within FOUR weeks after commencement of the III-Semester with the approval of the PEC.

12.3. Eligibility to appear for the semester-end examination:

12.3.1 A student shall be eligible to appear for semester-end examinations if he acquires a minimum of 75% of attendance in aggregate of all the courses in a semester.

12.3.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

12.3.3 Shortage of attendance below 65% in aggregate shall in no case be condoned.

12.3.4 Students whose shortage of attendance is not condoned in any semester shall not be eligible to take their semester-end examination and their registration shall stand cancelled.

12.3.5 A student shall not be promoted to the next semester unless he satisfies the attendance requirements of the semester, as applicable. The student may seek readmission for the semester when offered next. He will not be allowed to register for the courses of the semester while he is in detention.

12.3.6 A stipulated fee shall be payable to the college towards condonation of shortage of attendance.

12.4. Evaluation:

Following procedure governs the evaluation.

12.4.1. Marks for components evaluated internally by the faculty should be submitted to the Controller of Examinations one week before the commencement of the semester-end examinations. The marks for the internal evaluation components shall be added to the external evaluation marks secured in the semester-end examinations, to arrive at total marks for any course in that semester.

12.4.2. Performance in all the courses is tabulated course-wise and shall be scrutinized by the Results Committee and moderation is applied if needed and course-wise marks are finalized. Total marks obtained in each course are converted into letter grades.

12.4.3. Student-wise tabulation shall be done and individual grade sheet shall be generated and issued.

12.5. Personal verification / Revaluation / Recounting:

Students shall be permitted for personal verification/request for recounting/ revaluation of the semester-end examination answer scripts within a stipulated period after payment of prescribed fee. After recounting or revaluation, records shall be updated with changes if any and the student shall be issued a revised grade sheet. If there are no changes, the student shall be intimated the same through a notice.

12.6. Supplementary Examination:

In addition to the regular semester-end examinations conducted, the College may also schedule and conduct supplementary examinations for all the courses of other semesters when feasible for the benefit of students. Such of the candidates writing supplementary examinations may have to write more than one examination per day.

13. Re-Registration for Improvement of Internal Marks:

Following are the conditions to avail the benefit for improvement of internal evaluation marks.

13.1 The student should have completed all the course work and obtained examinations results for I,II and III semesters.

13.2 If the student has **failed** in the examination due to internal evaluation marks secured being less than 50%, he shall be given one chance for a maximum of 3 theory courses for improvement of internal evaluation marks.

13.3 The candidate has to register for the chosen courses and fulfill the academic requirements.

13.4 For each course, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D/ Challan in favour of the Principal, Sree Vidyanikethan Engineering College payable at Tirupati along with the requisition through the concerned Head of the Department.

13.5 If a student avails the benefit for Improvement of Internal evaluation marks, the internal evaluation marks as well as the semester-end examinations marks secured in the previous attempt(s) for the re-registered courses stands cancelled.

14. Academic Requirements for Completion of M.Tech degree Program:

The following academic requirements have to be satisfied in addition to the attendance requirements for completion of M.Tech degree Program.

14.1 A student shall be deemed to have satisfied the minimum academic requirements for each theory, laboratory and project work, if he secures not less than 40% of marks in the semester-end examination and a minimum of 50% of marks in the sum total of the internal evaluation and semester-end examination taken together. For the ***internship*** and ***open elective (MOOC) courses***, he should secure not less than 50% of marks in the semester-end examination.

14.2 A student shall register for all the 68credits and earn all the 68 credits. Marks obtained in the 68credits shall be considered for the calculation of the DIVISION based on CGPA.

14.3 A student who fails to earn 68credits as indicated in the curriculum within **four** academic years from the year of his admission shall forfeit his seat in M.Tech. Program and his admission stands cancelled.

15. Transitory Regulations:

Students who got detained for want of attendance (**or**) who have not fulfilled academic requirements (**or**) who have failed after having undergone the Program in earlier regulations (**or**) who have discontinued and wish to continue the Program are eligible for admission into the unfinished semester from the date of commencement of class work with the same (**or**) equivalent courses as and when courses are offered and they will be in the academic regulations into which they are presently readmitted.

A regular student has to satisfy all the eligibility requirements within the maximum stipulated period of **four years** for the award of M.Tech Degree.

16. Grades, Grade Point Average and Cumulative Grade Point Average:

16.1. Grade System: After all the components and sub-components of any course (including laboratory courses) are evaluated, the final total marks obtained shall be converted to letter grades on a "**10 point scale**" as described below.

Grades conversion and Grade points allotted

% of Marks obtained	Grade	Description of Grade	Grade Points (GP)
≥ 95	O	Outstanding	10
≥ 85 to < 95	S	Superior	9
≥ 75 to < 85	A	Excellent	8
≥ 65 to < 75	B	Very Good	7
≥ 55 to < 65	C	Good	6
≥ 50 to <55	D	Pass	5
< 50	F	Fail	0
Not Appeared	N	Absent	0

Pass Marks:

A student shall be declared to have passed theory course, laboratory course and project work if he secures minimum of 40% marks in Semester-end examination, and a minimum of 50% marks in the sum total of internal evaluation and Semester-end examination taken together. For the seminar, he shall be declared to have passed if he secures minimum of 50% of marks in the semester-end examinations. Otherwise he shall be awarded fail grade - **F** in such a course irrespective of internal marks. **F** is considered as a fail grade indicating that the student has to pass the semester-end examination in that course in future and obtain a grade other than **F** and **N** for passing the course.

16.2 Semester Grade Point Average (SGPA): SGPA shall be calculated as given below on a "10 point scale" as an index of the student's performance:

$$SGPA = \frac{\sum(C\ X\ GP)}{\sum C}$$

Where "C" denotes the "credits" assigned to the courses undertaken in that semester and "GP" denotes the "grade points" earned by the student in the respective courses.

Note: SGPA is calculated only for the candidates who appeared in the semester-end regular examinations in a particular semester:

16.3. Cumulative Grade Point Average (CGPA):

The CGPA shall be calculated for a candidate appeared in the Semester-end examinations for all the courses (including Regular & Supplementary) till that semester. The CGPA will be displayed in the Grade sheet of the Regular Semester-end examinations and also in the consolidated Grade Sheet issued at the end of the program. The CGPA is computed on a 10 point scale as given below:

$$CGPA = \frac{\sum(C\ X\ GP)}{\sum C}$$

where C denotes the credits assigned to courses undertaken up to the end of the Program and GP denotes the grade points earned by the student in the respective courses.

17. Grade Sheet: A grade sheet (Marks Memorandum) shall be issued to each student on his performance in all courses registered in that semester indicating the **SGPA and CGPA.**

18. Consolidated Grade Sheet: After successful completion of the entire Program of study, a Consolidated Grade Sheet indicating performance of all academic years shall be issued as a final record. Duplicate Consolidated Grade Sheet will also be issued, if required, after payment of requisite fee.

19. Award of Degree: The Degree shall be conferred and awarded by Jawaharlal Nehru Technological University Anantapur, Ananthapuramu on the recommendations of the Chairman, Academic Council, SVEC (Autonomous).

19.1. Eligibility: A student shall be eligible for the award of M.Tech Degree if he fulfills all the following conditions:

- Registered and successfully completed all the components prescribed in the Program of study to which he is admitted.
- Successfully acquired the minimum required credits as specified in the curriculum corresponding to the Program of study within the stipulated time.
- Obtained CGPA greater than or equal to 5.0 (Minimum requirement for declaring as passed).
- Has NO DUES to the College, Hostel, Library etc. and to any other amenities provided by the College.
- No disciplinary action is pending against him.

19.2. Award of Division: Declaration of division is based on CGPA.

Awarding of Division

CGPA	Division
> = 7.0	First Class with Distinction
> = 6.0 and < 7.0	First Class
> = 5.0 and < 6.0	Second Class

20. Additional Academic Regulations:

20.1 A student may appear for any number of supplementary examinations within the stipulated time to fulfill regulatory requirements for award of the degree.

20.2 In case of malpractice/improper conduct during the examinations, guidelines shall be followed as shown in the **ANNEXURE-I**.

20.3 When a student is absent for any examination (Mid-term or Semester-end) he shall be awarded **zero** marks in that component (course) and grading will be done accordingly.

20.4 When a component is cancelled as a penalty, he shall be awarded zero marks in that component.

21. Withholding of Results:

If the candidate has not paid dues to the College/University (or) if any case of indiscipline is pending against him, the result of the candidate shall be withheld and he will not be allowed/promoted to the next higher semester

22. Amendments to regulations:

The Academic Council of SVEC (Autonomous) reserves the right to revise, amend, or change the Regulations, Scheme of Examinations, and / or Syllabi or any other policy relevant to the needs of the society or industrial requirements etc., with the recommendations of the concerned Board(s) of Studies.

23. General:

The words such as "he", "him", "his" and "himself" shall be understood to include all students irrespective of gender connotation.

Note: *Failure to read and understand the regulations is not an excuse.*

ANNEXURE-I

GUIDELINES FOR DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

Rule No.	Nature of Malpractices/ Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the course of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester. The Hall Ticket of the candidate is to be cancelled.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including labs and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester. The candidate is also debarred for four consecutive semesters from class work and all Semester-end examinations, if his involvement is established. Otherwise, The candidate is debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course only.

6.	Refuses to obey the orders of the Chief Controller of Examinations/Controller of Examinations/any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the Controller of Examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the Controller of Examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester. If the candidate physically assaults the invigilator/Controller of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred for two consecutive semesters from class work and all Semester-end examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester. The candidate is also debarred and forfeits the seat.

Note: Whenever the performance of a student is cancelled in any course(s) due to Malpractice, he has to register for Semester-end Examinations in that course(s) consequently and has to fulfill all the norms required for the award of Degree.

Course Structure for M. Tech. (DECS)
SVEC-19

I-Semester

Sl. No.	Course Code	Course Title	Contact Periods per week				C	Scheme of Examinations Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1.	19MT13801	Advanced Digital Signal Processing	3	-	-	3	3	40	60	100
2.	19MT13802	Advanced Digital System Design	3	-	-	3	3	40	60	100
3.	19MT13803	Digital Communication Systems	3	-	-	3	3	40	60	100
Program Elective-1			3	-	-	3	3	40	60	100
4.	19MT15707	FPGA Architectures								
	19MT13804	Image and Video Processing								
	19MT13805	Information Theory and Coding Techniques								
Program Elective-2			3	-	-	3	3	40	60	100
5.	19MT15708	Low Power CMOS VLSI Design								
	19MT13806	Adaptive Signal Processing								
	19MT13807	RF Circuit Design & Microwave Devices								
6.	19MT10708	Research Methodology and IPR	2	-	-	2	2	40	60	100
7.	19MT13831	Advanced Digital System Design Lab	-	-	4	4	2	50	50	100
8.	19MT13832	Communications and Signal Processing Lab	-	-	4	4	2	50	50	100
Total			**17**	**-**	**8**	**25**	**21**	**340**	**460**	**800**
9.	19MT1AC01	Technical Report Writing	2	-	-	2	-	-	-	-

II-Semester

Sl. No.	Course Code	Course Title	Contact Periods per week				C	Scheme of Examinations Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1.	19MT23801	Advanced Wireless Communications	3	-	-	3	3	40	60	100
2.	19MT15706	VLSI Design Verification and Testing	3	-	-	3	3	40	60	100
Program Elective-3			3	-	-	3	3	40	60	100
3.	19MT25704	Memory Technologies								
	19MT23802	MIMO System								
	19MT23803	Speech Processing								
Program Elective-4			3	-	-	3	3	40	60	100
4.	19MT26305	Internet of Things								
	19MT25702	Physical Design Automation								
	19MT23804	Software Defined Radio								
	19MT2MOOC	Open Elective (MOOC)	-	-	-	-	3	-	100	100
5.	19MT23831	Advanced Communications Lab	-	-	4	4	2	50	50	100
6.	19MT23832	VLSI Design Verification and Testing Lab	-	-	4	4	2	50	50	100
Total			**12**	**-**	**8**	**20**	**19**	**260**	**440**	**700**
7.	19MT2AC01	Statistics with R	2	-	-	2	-	-	-	-

III-Semester

Sl. No.	Course Code	Course Title	Contact Periods per week				C	Scheme of Examinations Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
5.	19MT33831	Internship	-	-	-	-	2	-	100	100
6.	19MT33832	Project Work Phase-I	-	-	20	20	10	50	50	100
Total			**-**	**-**	**20**	**20**	**12**	**50**	**150**	**200**

IV-Semester

Sl. No.	Course Code	Course Title	Contact Periods per week				C	Scheme of Examinations Max. Marks		
			L	T	P	Total		Int. Marks	Ext. Marks	Total Marks
1.	19MT43831	Project Work Phase-II	-	-	32	32	16	150	150	300
Total			**-**	**-**	**32**	**32**	**16**	**150**	**150**	**300**
Total Credits							**68**	**-**	**--**	**--**
Grand Total Marks:										**2000**

M.Tech. - I Semester
(19MT13801) ADVANCED DIGITAL SIGNAL PROCESSING
(Common to DECS & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Course on Digital Signal Processing at UG level

COURSE DESCRIPTION:

Digital filter banks; Parametric and Non-Parametric Power Spectrum Estimation methods; computationally efficient algorithms; Applications of DSP.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in Digital Signal Processing and applications
CEO2: To develop skills in design, analysis, problem solving and research in Multirate Signal Processing, Linear prediction, Power Spectral Estimation and Communications.

COURSE OUTCOMES:

After successful completion of the course, student will be able to:

CO1: Analyze sampling rate conversion, various DSP algorithms and design digital Filter Banks to improve performance characteristics of digital systems in multidisciplinary environments like image processing, wireless communication, biomedical engineering, speech processing, video processing, etc
CO2: Realize, compare and estimate power spectrum using different Non-Parametric and Parametric Methods in the frequency analysis of systems.
CO3: Understand Linear Prediction, analyze Lattice Forward and Backward Predictors for Radar signal Processing and Remote sensing.
CO4: Apply signal processing techniques in fields such as communications, speech processing, Image and video processing.

DETAILED SYLLABUS:

Unit-I: Multirate Filter Banks (Hours: 10)
Decimation, Interpolation, Sampling rate conversion by a rational factor I/D, Multistage Implementation of sampling rate conversion. **Digital Filter Banks**: Two-Channel Quadrature-Mirror Filter Bank, Elimination of aliasing, condition for Perfect Reconstruction, Polyphase form of QMF bank, Linear phase FIR QMF bank, IIR QMF bank, Perfect Reconstruction Two-Channel FIR QMF Bank.

Unit-II: DSP Algorithms (Hours: 08)
Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier Transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

Unit-III: Power Spectral Estimations (Hours: 09)
Estimation of spectra from finite duration observation of signals.
Non-Parametric Methods: Bartlett, Welch, Blackman & Tukey methods. Performance Characteristics of Non-parametric Power Spectrum Estimators, Computational Requirements of Non-parametric Power Spectrum Estimates.

Parametric Methods of Power Spectral Estimation:
Auto correlation & Its Properties, Relationship between auto correlation & model parameters, Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation.

Unit-IV: Linear Prediction (Hours: 08)
Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters.

Unit-V: Applications of Digital Signal Processing (Hours: 10)
Digital cellular mobile telephony, Adaptive telephone echo cancellation, High quality A/D conversion for digital Audio, Efficient D/A conversion in compact hi-fi systems, Acquisition of high quality data, Multirate narrow band digital filtering, High resolution narrow band spectral analysis.

Total Hours: 45

TEXT BOOKS:

1. John G. Proakis, Dimitris G. Manolakis, "*Digital signal processing, principles, Algorithms and applications",* Prentice Hall, 4th edition, 2007.
2. Sanjit K Mitra, "*Digital signal processing, A computer base approach",* McGraw-Hill Higher Education, 4th edition, 2011.

REFERENCE BOOKS:

1. Emmanuel C Ifeacher Barrie. W. Jervis, "*DSP-A Practical Approach*", Pearson Education, 2nd edition, 2002.
2. A.V. Oppenheim and R.W. Schaffer, "*Discrete Time Signal Processing",* PHI, 2nd edition, 2006.

M.Tech. - I Semester
(19MT13802) ADVANCED DIGITAL SYSTEM DESIGN

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Switching Theory and Logic Design at UG Level.

COURSE DESCRIPTION:

ASM Charts; Fault Modelling; Fault Diagnosis; PLA minimization; cycles and hazards

COURSE OBJECTIVES:

CEO1: To impart the knowledge in identifying various faults, test generation algorithms, PLD'S, BIST.
CEO2: To develop skills in analyzing, design of complex digital systems and solve different engineering problems.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Design digital systems using ASM Charts, ROMs, PLAs, CPLDs and FPGAs and modeling them in HDL.
CO2: Classify Fault Models and diagnose the Combinational Circuits using Conventional Methods.
CO3: Use appropriate approaches to Perform Fault diagnosis of Sequential Circuits.
CO4: Model faults in Programmable Logic Arrays, apply appropriate methods to Minimize and test them.
CO5: Apply Appropriate Methods to reduce incompletely specified machines and overcome races, hazards and cycles.

DETAILED SYLLABUS:

Unit-I: Design of Digital Systems (Hours: 09)
ASM charts, Hardware description language and control sequence method, Design of Iterative circuits, Design of sequential circuits using ROMs, PLAs, CPLDs and FPGAs.

Unit-II: Fault Modeling & Test Pattern Generation (Hours: 10)
Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults. Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm, D - algorithm, PODEM, Signature Analysis and testing for bridging faults.

Unit-III: Fault Diagnosis in Sequential Circuits (Hours: 08)
Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Unit-IV: PLA Minimization and Testing (Hours: 09)
PLA minimization - PLA folding. Fault model in PLA, Test generation and Testable PLA design.

Unit-V: Asynchronous Sequential Machines (Hours: 09)
Fundamental-mode model, The flow table, Reduction of incompletely specified Machines, races, cycles and hazards.

Total Hours: 45

TEXT BOOKS:

1. Charles H. Roth, Jr., "*Fundamentals of Logic Design*", Cengage Learning, 5th edition, 2004.
2. N. N. Biswas, "*Logic Design Theory*", PHI, 1993.

REFRENCE BOOKS:

1. Samuel C. Lee, *"Digital Circuits and Logic Design"*, PHI, 1976.
2. Norman Balabanian, Bradley Carlson, "*Digital Logic Design Principles*", John Wily & Sons, Inc., 2002.
3. Parag K. Lala,*"Fault Tolerant and Fault Testable Hardware Design*", BS Publications, 1990.

M.Tech. - I Semester
(19MT13803) DIGITAL COMMUNICATION SYSTEMS
(Common to DECS & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES: --

A Course on Digital Communications at UG Level**,** Review of random Variables and Processes

COURSE DESCRIPTION:

Band pass signals and systems; Digital modulation techniques; Design of optimum receivers; Generation and detection of spread spectrum signals.

COURSE OBJECTIVES:

CEO1: To impart knowledge on Characterizing and analyzing the Communication Signals and Systems, Digital modulation techniques and Communication over AWGN channels
CEO2: To design optimum Receivers for the Additive Gaussian Noise Channel and Solve the problems in Spread Spectrum Technique and Multichannel and Multicarrier Systems Digital Modulation Techniques;

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1 : Demonstrate in-depth knowledge on response of systems for Band Pass, signal space and multidimensional representations of signals.
CO2 : Analyze various digital Modulation Techniques to improve the performance of digital communication systems.
CO3 : Analyze the performance of optimum receiver for Signals with Random Phase in AWGN Channel.
CO4 : Apply Spread Spectrum techniques in Anti jamming Application, Low-Detectability Signal Transmission and Code Division Multiple Access.
CO5 : Analyze the performance of Multichannel and Multicarrier systems.

DETAILED SYLLABUS:

Unit-I: Characterization of Communication Signals and Systems (Hours: 09)
Representation of Band Pass Signals and Systems–Representation of Band Pass Signals, Representation of Linear Band-Pass System, Response of a Band-Pass System to a Band-Pass Signal. Signal Space Representations – Vector Space Concepts, Signal Space Concepts, Orthogonal Expansion of Signals. Representation of Digitally Modulated Signals – Memory Less Modulation Methods – PAM Signals, Phase Modulated Signals, QAM Signals, Multidimensional Signals, Orthogonal Multidimensional Signals.

Unit-II: Digital Modulation Techniques (Hours: 09)
Digital Modulation – Factors that Influence the Choice of Digital Modulation, Bandwidth and Power Spectral Density of Digital Signals. Linear Modulation Techniques – BPSK, DPSK, QPSK, OQPSK, Π/4 QPSK. Constant Envelope Modulation Techniques – MSK, GMSK, Combined Linear and Constant Envelope Modulation Techniques – M-ary PSK, M-ary QAM.

Unit-III: Optimum Receivers for the Additive Gaussian Noise Channel

(Hours: 09)

Optimum Receiver for Signals corrupted by AWGN –Correlation demodulator, Matched Filter Demodulator, Optimum Detector. Performance of the Optimum Receiver for Memory Less Modulation – Probability of Error for Binary Modulation, M-ary Orthogonal Signals, M-ary PAM, M-ary PSK, QAM. Optimum Receiver for Signals with Random Phase in AWGN Channel – Optimum Receiver for Binary Signals, Optimum Receiver for M-ary Orthogonal Signals.

Unit-IV: Spread Spectrum Techniques (Hours: 09)

Introduction, Model of Spread Spectrum Digital Communication System, Direct Sequence Spread Spectrum Signals – Introduction, The Processing Gain and Jamming Margin. Applications of Direct Sequence Spread Spectrum Signals – Anti jamming Application, Low-Detectability Signal Transmission, Code Division Multiple Access. Generation of PN-Sequences, Frequency-Hopped Spread Spectrum Signals, Other Types of Spread Spectrum Signals. Detection of spread spectrum signals- Matched filter receiver.

Unit-V: Multichannel and Multicarrier Systems (Hours: 09)

Rayleigh and Rician channels, Multichannel Digital Communications in AWGN Channels; Binary Signals, M-ary Orthogonal Signals. Multicarrier Communications; Single Carrier verses Multicarrier Modulation, Capacity of a Non ideal Linear Filter Channel, OFDM, Modulation & Demodulation in an OFDM.

Total Hours: 45

TEXT BOOKS:

1. John G. Proakis, "*Digital Communications*", McGraw-Hill, 4th edition, 2001.
2. Theodore S. Rappaport, "*Wireless Communications*", Pearson Education, 2nd edition, 2002.

REFERENCE BOOKS:

1. Marvin K. Simon, Jim K Omura, Robert A. Scholtz & Barry K.Levit, "*Spread Spectrum Communications*", McGraw-Hill, 1st edition,1995.
2. J.Marvin, K.Simon, Sami. M.Hinedi and William C. Lindsey, "*Digital Communication Techniques*", PHI, 2009.
3. George R. Cooper & Clare D. McGillem, "*Modern Communication and Spread Spectrum*", McGraw-Hill Book Company, 1986.
4. K. Fazel and S. Kaiser, "*Multi-Carrier and Spread Spectrum Systems*", A John Wiley and Sons, Ltd, Publication, 2nd edition, 2008.

ADDITIONAL LEARNING RESOURCES

1. https://nptel.ac.in/courses/108102096/
2. https://onlinecourses.nptel.ac.in/noc17_ec12/
3. https://nptel.ac.in/courses/117105144/
4. https://nptel.ac.in/courses/117105144/5

M.Tech. - I Semester
(19MT15707) FPGA ARCHITECTURES
(Common to DECS & VLSI)
(Program Elective-1)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Digital Logic Design and VLSI Design at UG Level.

COURSE DESCRIPTION:

Evolution of Programmable Devices, Xilinx, Actel, Altera FPGAs, Logic Synthesis, Technology Mapping, Finite State Machines, Realizations of SM Charts, One Hot Method, System level Design, Device Applications-Fast Bus Controller, FIFO Controller & Intelligent I/O Subsystem

COURSE OBJECTIVES:

CEO1. To impart knowledge in architectures and applications of various families of CPLDs and FPGAs.
CEO2. To develop skills in design, analysis and problem solving for implementation and verification of functions in CPLDs/FPGAs.
CEO3. Apply knowledge and skills for performance analysis in the design of FSMs.

COURSE OUTCOMES:

After successful completion of the course, student will be able to:

CO1. Analyze the placement and routing architectures of different programmable gate arrays to improve performance characteristics of digital systems
CO2. Realize, compare and estimate the technology mapping issues in CPLDs and FPGAs.
CO3. Understand state machine charts and its realizations to evaluate the performance of device applications.
CO4. Analyze various FSM architectures and system level design.
CO5. Understand various device applications used in communications, speech processing, Image and video processing.

DETAILED SYLLABUS:

Unit - I: Introduction to Programmable Logic and FPGAs (Hours: 08)
Evolution of Programmable Devices, CPLD Altera Series Max 5000, MAX 7000 Series. Field Programmable Gate Arrays –Design Flow, Placement , Routing Architecture. Altera FPGAs. Advanced Micro Devices (AMD) FPGA. Applications of FPGAs.

Unit - II: (Hours: 09)
Xillinx and Actel FPGAs :
Case Studies – Xilinx XC2000, XilinxXC3000, Xilinx 4000 FPGAS. Actel FPGAs- Actel ACT1, Actel ACT2 , Actel ACT3.
Technolgoy Mapping for FPGAs: Logic Synthesis. Lookup Table Technology, Mapping Multiplexer Technology Mapping- The Proserphine Technology Mapper, Multiplexers Technology Mapping in Mis pga, A map and XA map Technology Mappers.

Unit - III: Finite State Machine (Hours: 09)
Finite State Machines, State Transition Table, State Assignment for FPGAs, Hazards and One Hot Encoding. Mustang. State Machine Charts, Derivations of State Machine Charges, Realization of State Machine Charts.

Unit - IV: FSM Architectures and System Level Design (Hours: 10)
Architectures Centered Around Non Registered PLDs, State Machine Designs Centered Around Shift Registers, One – Hot Design Method, Use of ASMs in One Hot Design, Application of One Hot Method. System Level Design – Controller, Data Path and Functional Partition.

Unit - V: Device Applications (Hours: 09)
MAX 5000 Timing, Using Expanders to Build Registered Logic in MAX EPLDs, Simulating Internal Buses in General Purpose EPLDs, Fast Bus Controllers with EPM5016, Micro Channel Bus Master and SDP Logic with the EPM5032 EPLD, FIFO Controller Using an EPM7096, Integrating an Intelligent I/O Subsystem with a Single EPM5130 EPLD.

Total Hours: 45

TEXT BOOKS:

1. S.Brown, R.Francis, J.Rose, Z.Vransic, "*Field Programmable Gate Array*", Kluwer Publication, 1992.
2. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall (PTE), 1994
3. Richard Tinder, "*Engineering Digital Design*", Academic Press, 2nd Edition, 2000.

REFERENCE BOOKS:

1. Charles H. Roth, Jr, "*Fundamentals of Logic Design*", Cengage Learning, 5th Edition, 2004.
2. S.Trimberger, Edr., "*Field Programmable Gate Array Technology*", Kluwer Academic Publications, 1994.

M.Tech. – I/II Semester
(19MT13804) IMAGE & VIDEO PROCESSING
(Common to DECS & CMS)
(Program Elective-1)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Digital Communications & Digital Signal Processing at UG Level

COURSE OBJECTIVES:

CEO1: To impart knowledge in fundamentals that helps in developing various algorithms pertaining to Image and Video Processing.
CEO2: To attain skills required for analysis, design and problem solving by the use of techniques required for modeling of image and video processing.
CEO3: To inculcate attitude for providing solutions for societal use in the area of image and video processing.

COURSE OUTCOMES:

After completion of this course, student will be able to:

CO1: Apply sampling, quantization, transformation and filtering techniques on image & video.
CO2: Analyze Image enhancement, restoration, segmentation techniques for improving visual quality of image
CO3: Analyze compression techniques to reduce the storage capacity of image
CO4: Develop three dimensional motion models, motion estimation methods and filtering techniques in video processing.

DETAILED SYLLABUS

Unit-I: Fundamentals of Image Processing and Image Transforms (Hours: 07)
Fundamental steps in Image Processing, Gray scale and color Images, image sampling and quantization, **2-D Transforms:** DFT,Walsh, Hadamard, Haar, KLT, DCT.

Unit-II: Image Enhancement & Restoration (Hours: 09)
Enhancement: Intensity transformation functions, Filters in spatial and frequency domains, histogram processing, homomorphic filtering.
Restoration: Image Degradation Model, Restoration in presence of noise only- spatial filtering, inverse filtering, Wiener filtering and Constrained least squares filtering.

Unit-III: Image Compression & Image Segmentation (Hours: 09)
Image compression fundamentals -Redundancies, Compression models: Lossy & Lossless Predictive coding, Arithmetic coding, Bit plane coding, Run length coding, symbol based coding, Transform coding, Digital Watermarking.
Segmentation: Fundamentals, Point, line and edge detection, Thresholding, Region based segmentation.

Unit-IV: Video Processing- I (Hours: 10)
Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling for Analog and Digital Video, Two-Dimensional Rectangular Sampling, Two-Dimensional Periodic Sampling, Sampling on 3-D Structures, Reconstruction from Samples.

Unit-V: Video Processing –II **(Hours: 10)**

Motion Estimation: 2-D Motion vs. Apparent Motion, 2-D Motion Estimation, Methods Using the Optical Flow Equation. Video filtering: motion compensated filtering, noise filtering, restoration, video compression standards.

Total Hours: 45

TEXT BOOKS:

1. "*Digital Image Processing*", Gonzalez and Woods, 3rd ed., Pearson Education, 2008.
2. A. M. Tekalp, "*Digital Video Processing*", Prentice-Hall, 1995.

REFERENCE BOOK:

1. Anil K. Jain, "Fundamentals of Digital Image Processing", Pearson Education, Inc., 2002.

M.Tech. - I Semester
(19MT13805) INFORMATION THEORY AND CODING TECHNIQUES
(Program Elective-1)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Digital Communications at UG Level

COURSE OBJECTIVES:

CEO1: To impart knowledge in Various aspects of Entropy, Channel capacity, source and Channel coding techniques, Performance evaluation of various source coding technique
CEO2: To develop skills in design, analysis and problem solving related to Channel Capacity and Channel coding techniques.
CEO3: Apply knowledge and skills for performance analysis of digital systems using Linear Block Codes, Convolution Codes, BCH codes, RS Codes etc.

COURSE OUTCOMES:

After successful completion of the course, student will be able to:

CO1: Analyze Differential Entropies, mutual information and lossless source codes to improve Error performance characteristics of digital systems in environments like wireless communication, Digital audio and video processing systems.
CO2: Analyze channel capacity using channel codind theorems in Gaussian channels.
CO3: Analyze various Channel Coding Techniques for Error Detection and correction in signal processing and communications.

DETAILED SYLLABUS

Unit-I: Introduction (Hours: 09)
Entropy: Discrete stationary sources, Markov sources, Entropy of a discrete Random variable- Joint, conditional, relative entropy, Mutual Information and conditional mutual information. Chain rules for entropy, relative entropy and mutual information, Differential Entropy- Joint, relative, conditional differential entropy and Mutual information.
Loss less Source coding: Uniquely decodable codes, Instantaneous codes, Kraft's inequality, optimal codes, Huffman code, Shannon's Source Coding Theorem, Examples of Source Coding- Audio Compression, Image Compression

Unit-II: Channel Capacity (Hours: 08)
Capacity computation for some simple channels, Channel Coding Theorem, Fano's inequality and the converse to the Coding Theorem, Equality in the converse to the coding theorem, The joint source Channel Coding Theorem, The Gaussian channels- Capacity calculation for Band limited Gaussian channels, Parallel Gaussian Channels, Capacity of channels with colored Gaussian noise.

Unit-III: Channel Coding-1 (Hours: 08)
Linear Block Codes: Introduction to Linear block codes, Generator Matrix, Systematic Linear Block codes, , Parity Check Matrix, Syndrome testing, Error correction, Decoder Implementation of Linear Block Codes, Error Detecting and correcting capability of Linear Block codes.

Unit-IV: Channel Coding-2 **(Hours: 11)**

Cyclic Codes: Algebraic Structure of Cyclic Codes, Binary Cyclic Code Properties, Encoding in Systematic Form, Systematic Encoding with an (n - k)-Stage Shift Register, Error Detection with an (n - k)-Stage Shift Register, Well-Known Block Codes-Hamming Codes, Extended Golay Code, BCH Codes.

Convolutional Codes: Convolution Encoding, Convolutional Encoder Representation, Formulation of the Convolutional Decoding Problem, Properties of Convolutional Codes, Sequential Decoding.

Unit-V: Channel Coding-3 **(Hours: 09)**

Reed-Solomon Codes- Reed-Solomon Error Probability, Finite Fields, Reed-Solomon Encoding, Reed-Solomon Decoding, Interleaving and Concatenated Codes- Block Interleaving, Convolutional Interleaving, Concatenated Codes. Coding and Interleaving Applied to the Compact Disc Digital Audio System- CIRC Encoding, CIRC Decoding. Turbo Codes-Turbo Code Concepts, Encoding with Recursive Systematic Codes, Feedback Decoder, The MAP Decoding Algorithm.

Total Hours: 45

TEXT BOOKS:

1. Thomas M. Cover and Joy A. Thomas, "*Elements of Information Theory*", John Wiley & Sons, 1st edition, 1999.
2. Bernard sklar, "*Digital Communications–Fundamental and Application*", Pearson Education, 2nd edition, 2009.

REFERENCE BOOKS:

1. Robert Gallager, "*Information Theory and Reliable Communication*", John Wiley & Sons, 1st edition, 1968.
2. John G. Proakis, "*Digital Communications*", Mc. Graw Hill Publication, 5th edition, 2008.
3. Shulin and Daniel. Costello, Jr., "*Error Control Coding–Fundamentals and Applications*", Prentice Hall, 2nd edition, 2002.

ADDITIONAL LEARNING RESOURCES

1. Robert G. Gallager, "*Information Theory and Reliable Communications*'', John Wiley & Sons, 1968.
2. Raymond W. Yeung, "*Information Theory and Network Coding*'', Springer, 2008.
3. David J. C. MacKay, "*Information Theory, Inference, and Learning Algorithms*'', Cambridge University Press.
4. Robert Ash, "*Information Theory*'', Dover Publications, 1965.
5. Imre Csiszar and Jonos Korner, "*Information Theory*'', 2nd edition, Cambridge University Press, 2011.

M.Tech. - I Semester
(19MT15708) LOW POWER CMOS VLSI DESIGN
(Common to DECS & VLSI)
(Program Elective-2)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on VLSI Design at UG Level

COURSE DESCRIPTION:

Need for low power VLSI chips, Sources of Power dissipation in MOS & CMOS Devices, Power Estimation, Synthesis of low power VLSI Circuits, Design of low power VLSI Circuits, Low power Memory Architectures, Energy recovery Circuits, Software design of low power VLSI Circuits.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in low power CMOS Circuits.
CEO2: To develop skills in design, analysis and problem solving related to high performance and low power devices.
CEO3: Apply knowledge and skills pertaining to low voltage CMOS circuit design for for wide range of IC applications.

COURSE OUTCOMES:
After successful completion of the course, student will be able to:

CO1: Analyze the various power dissipation effects and estimation methods in CMOS VLSI Circuits to improve the performance characteristics of digital systems.
CO2: Understand the various design styles and synthesis of low power and low voltage CMOS VLSI circuits.
CO3: Analyze the various low power Static RAM architectures in design and development of Ultra Low power Integrated Circuits.
CO4: Apply energy recovery techniques to evaluate the performance of low power VLSI Circuits for scientific research in design and development of digital systems.

DETAILED SYLLABUS:

Unit –I (Hours: 07)
Power Dissipation in CMOS VLSI design: Need for low power VLSI chips, Sources of Power dissipation , Power dissipation in MOS & CMOS Devices, Limitations of low Power design.

Unit –II (Hours: 08)
Power Estimation: Modeling of Signals, Signal Probability Calculation, Probabilistic Techniques for Signal activity Estimation, Statistical Techniques, Estimation of Glitching Power, Sensitivity Analysis, Power Estimation using input vector Compaction, Estimation of Maximum Power.

Unit-III (Hours: 10)
Synthesis for Low Power: Behavioral Level Transforms, Logic Level optimization of low power, Circuit level.
Design and Test of Low Voltage CMOS Circuits: Circuit Design Style, Leakage current in Deep Sub micrometer Transistors, Low voltage Circuit Design Techniques, Multiple Supply Voltages.

Unit-IV **(Hours: 10)**

Low Power Static RAM Architectures: Organization of Static RAM, MOS Static RAM Memory Cell, Banked Organization of SRAMs, Reducing Voltage Swing in Bit lines, Reducing Power in Sense Amplifier Circuits.

Unit-V **(Hours: 10)**

Low Energy Computing using Energy Recovery Techniques: Energy Recovery Circuit Design, Designs with partially Reversible logic, Supply Clock Generation.

Software design for low power: Sources of software power dissipation, software power estimation, Software power estimation, Co-design for low power.

Total Hours: 45

TEXT BOOK:

1. Kaushik Roy, Sharat Prasad, *"Low-Power CMOS VLSI Circuit Design"* Wiley Student Edition, 2000.

REFERENCE BOOK:

1. Kiat-Seng Yeo, Samir S.Rofail and Wang-Ling Goh, *"CMOS/BiCMOS ULSI: Low power, Low Voltage "*, Pearson education, 2002.

M.Tech. - I Semester
(19MT13806) ADAPTIVE SIGNAL PROCESSING
(Common to DECS & CMS)
(Program Elective-2)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on Signal Processing at UG Level

COURSE DESCRIPTION:

Development of adaptive filter theory; Method of steepest descent;Least-Mean-Square Algorithm and recursive least square algorithm; Kalman filtering algorithm; order - recursive adaptive filters.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in various adaptive algorithms for designing optimal filters.
CEO2: To analyze, design and implement adaptive filters using LMS, RLS and Kalman filtering algorithms for solving problems in the fields of signal processing, communications, Bio- Medical, Instrumentation and control engineering.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Understand linear optimum and adaptive filters to determine mean square error.
CO2: Analyze Steepest-Descent Algorithm and apply to the wiener filters.
CO3: Solve problems in the error minimization using LMS and RLS Algorithms.
CO4: Develop kalman and non Linear adaptive filters in the fields of signal processing, communications, Bio-Medical, Instrumentation and control engineering for optimization.
CO5: Analyze adaptive forward and backward linear prediction.

DETAILED SYLLABUS:

Unit-I: Introduction to Adaptive Systems & Development of Adaptive Filter Theory (Hours: 10)

Eigen Value Problem, Properties of eigen values and eigen vectors(proof is not required), Eigen Filters, eigen Value computations. The Filtering problem,Linear Optimum Filters, Adaptive Filters, Linear Filter sturucters, Approaches to the development of linear adaptive filters. Linear Optimum Filtering: Statement of the problem, Principle of Orthogonality, Minimum Mean Square Error, Wiener- Hopf equations, Error- Performance Surface.

Unit-II: Method of Steepest Descent (Hours: 07)

Basic Idea of Steepest-Descent Algorithm, Steepest-Descent Algorithm applied to the Wiener Filter, Stability of the Steepest-Descent Algorithm, Examination of the transient behavior of the Steepest-Descent Algorithm, the Steepest-Descent Algorithm as a deterministic search method, Virtue and limitation of the Steepest-Descent Algorithm.

Unit-III: Least-Mean-Square Adaptive Filters and Recursive Least-Squares Adaptive Filters (Hours: 10)

Overview of the structure and operation of the Least-Mean-Square Algorithm, Least-Mean-Square adaptation Algorithm, Applications-Adaptive Noise cancelling Applied to a Sinusoidal Interference and Adaptive Beam forming, Comparison of the LMS Algorithm with Steepest-Descent Algorithm.

Matrix Inversion lemma, exponentially weighted recursive least square algorithm, update recursion for the sum of weighted error squares, Single-Weight Adaptive Noise Canceller convergence analysis of RLS Algorithm.

Unit-IV: Kalman Filtering & Non Linear Adaptive Filtering (Hours: 10)

Recursive Minimum Mean-Square Estimation for Scalar Random variables, Statement of Kalman filtering problem, The Innovations Process, estimation of the state using the Innovations Process, Filtering, Initial conditions.

An overview of the Blind Deconvolution problem, Buss Gang Algorithm for blind Equalization.

Unit-V: Order-Recursive Adaptive Filters (Hours: 08)

Gradient-Adaptive Lattice Filter, order-recursive adaptive filters using least square estimation, adaptive forward linear prediction, adaptive backward linear prediction, conversion factor, least-square lattice predictor, angle-normalized estimation errors, first order state space models for lattice filtering.

Total Hours: 45

TEXT BOOK:

1. Simon Haykin, *"Adaptive Filter Theory",* Pearson Education, 4th edition, 2002.

REFERENCE BOOK:

1. Bernard Widrow, Samuel D. Strearns, *"Adaptive Signal Processing",* Pearson Education, 1985.

M.Tech. - I Semester
(19MT13807) RF CIRCUIT DESIGN & MICROWAVE DEVICES
(Common to DECS & CMS)
(Program Elective-2)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Concept of Basic Electronics and Wave Theory at UG level

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in the fields of RF Circuits.
CEO2: To develop skills in analytical, problem solving, design and application skills in the broad area of RF circuit design.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Understand and apply the basic concepts of RF Electronics, analyze transmission lines, matching and biasing networks, and RF components, Design RF devices in Wireless Communications.
CO2: Realize, compare, and estimate problems in RF Passive and Active components as well as smart antenna techniques in the field of RF Circuits.
CO3: Analyze RF circuits and demonstrates use of Smith Chart for high frequency circuit design.
CO4: Apply techniques like MF-UHF for designing high-power microstrip circuits, directional couplers, transformers, composite and multilayer inductors, filters, combiners/dividers, and RFID systems in the field of wireless communication systems.
CO5: Analyze noise in RF devices like Oscillators, and synthesizers.

DETAILED SYLLABUS:

Unit-I: Introduction to RF Electronics (Hours: 09)
The Electromagnetic Spectrum, units and Physical Constants, Microwave bands, RF behavior of Passive components: Tuned resonant circuits, Vectors, Inductors and Capacitors. Voltage and Current in capacitor circuits, Tuned RF / IF Transformers.

Unit-II: Transmission Line Analysis (Hours: 12)
Examples of transmission lines, Transmission line equations and Biasing: Kirchoffs Voltage and current law representation, Traveling voltage and current waves, General Impedance definition, lossless transmission line model. Micro Strip Transmission Lines, Special Termination Conditions, sourced and Loaded Transmission Lines.
Single and Multiport Networks: The Smith Chart, Interconnectivity networks, Network properties and Applications, Scattering Parameters.

Unit-III: Microwave Components (Hours: 08)
Microwave resonators, Microwave filters, power dividers and directional couplers, Ferromagnetic devices and components.
Nonlinearity and Time Variance Inter-symbol interference, random process & noise, definition of sensitivity and dynamic range, conversion gain and distortion.

Unit-IV: Microwave Semiconductor Devices and Modeling (Hours: 08)
PIN diode, Tunnel diodes, Varactor diode, Schottky diode, IMPATT and TRAPATT devices, transferred electron devices, Microwave BJTs, GaAs FETs, low noise and power GaAs FETs, MESFET, MOSFET, HEMT.

Unit-V: Oscillators and Mixers (Hours: 08)
Oscillator basics, Low phase noise oscillator design, High frequency Oscillator configuration, LC Oscillators, VCOs, Crystal Oscillators, PLL Synthesizer, and Direct Digital Synthesizer.
RF Mixers: Basic characteristics of a mixer, Active mixers, Image Reject and Harmonic mixers, Frequency domain considerations.

Total Hours: 45

TEXT BOOKS:

1. Reinhold Ludwing, Pavel Bretchko, "*RF Circuit design: Theory and applications*", Pearson Education Asia Publication, 1st edition, New Delhi 2001.
2. D.M.Pozar, "*Microwave engineering*", Wiley, 4th edition, 2011.
3. Matthew M. Radmanesh, "*Advanced RF & Microwave Circuit Design: The Ultimate Guide to Superior Design*", Author House, 1st edition, 2009.

REFERENCE BOOKS:

1. Devendra K. Misra, "*Radio Frequency and Microwave Communication Circuits – Analysis and Design*", Wiley Student Edition, John Wiley & Sons, 2nd edition, July 2004.
2. Christopher Bowick, Cheryl Aljuni and John Biyler, "*RF Circuit Design*", Elsevier Science, 2nd edition, 2007.
3. S.Y. Liao, "*Microwave circuit Analysis and Amplifier Design*", Prentice Hall, 1st edition 1987.
4. Radmanesh, "*RF and Microwave Electronics Illustrated*", Pearson Education, 1st edition, 2004.

ADDITIONAL LEARNING RESOURCES

https://nptel.ac.in/courses/117102012/

M. Tech.-I Semester
(19MT10708) RESEARCH METHODOLOGY AND IPR

(Common to all M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	2	-	-	2

PRE REQUISITES:

COURSE DESCRIPTION:

Overview of research; research problem and design; various research designs; Data collection methods; Statistical methods for research;Interpretation& drafting reports and Intellectual property rights.

COURSE OBJECTIVES:

CEO1. To impart knowledge on research methodology and subsequent process involved for successful accomplishment of the research.
CEO2. To impart knowledge on intellectual property rightsand subsequent process involved infiling patents and trade mark registration process.
CEO3. To inculcate attitude of reflective learning and contribute to the society through fruitful research.

COURSE OUTCOMES:

On successful completion of the course, student will be able to:

CO1. Apply the conceptual knowledge of research methodology to formulate the hypothesis, data collection and processing, analyzing the data using statistical methods, interpret the observations and communicating the novel findings through a research report.
CO2. Practice ethics and have responsibility towards society throughout the research process and indulge in continuous learning process.
CO3. Apply the conceptual knowledge of intellectual property rights for filing patents and trade mark registration process.

DETAILED SYLLABUS:

Unit-I: Introduction to Research Methodology (Hours: 07)
Objectives and Motivation of Research, Types of Research, Defining and Formulating the Research Problem; Features of research design, Different Research Designs; Different Methods of Data Collection, Data preparation and Processing.

Unit-II: Data Analysis and Hypothesis Testing (Hours: 09)
ANOVA; Principles of least squares-Regression and correlation; Normal Distribution-Properties of Normal Distribution; Testing of Hypothesis–Hypothesis Testing Procedure, Types of errors, t-Distribution, Chi-Square Test as a Test of Goodness of Fit.

Unit-III: Interpretation and Report Writing (Hours: 04)
Interpretation – Need, Techniques and Precautions; Report Writing – Significance, Different Steps, Layout, Types of reports,Mechanics of Writing a Research Report, Precautions in Writing Reports; Research ethics.

Unit-Iv: Introduction to Intellectual property and Trade Marks (Hours: 07)
Importance of intellectual property rights; types of intellectual property, international organizations; Purpose and function of trademarks, acquisition of trade mark rights, protectable matter, selecting and evaluating trade mark, trade mark registration processes.

Unit-V: Law of Copyrights **(Hours: 08)**

Fundamental of copy right law, originality of material, rights of reproduction, rights to perform the work publicly, copy right ownership issues, copy right registration, notice of copy right, international copy right law.

Law of patents: Foundation of patent law, patent searching process, ownership rights and transfer

New Developments in IPR: Administration of Patent System.

Total Hours: 35

TEXT BOOKS:

1. C.R. Kothari, *Research Methodology: Methods and Techniques*, 2nd revised edition, New Age International Publishers, New Delhi, 2004.
2. Deborah, E. Bouchoux, *Intellectual property right*, 5th edition, Cengage learning, 2017.

REFERENCE BOOKS:

1. R. Panneerselvam, *Research Methodology*, PHI learning Pvt. Ltd., 2009.
2. Prabuddha Ganguli, *Intellectual property right - Unleashing the knowledge economy*, Tata McGraw Hill Publishing Company Ltd, 2001.

M.Tech. - I Semester
(19MT13831) ADVANCED DIGITAL SYSTEM DESIGN LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES: A Course on Digital Design at UG Level

COURSE OBJECTIVS:

CEO1: To acquire knowledge on Combinational, Sequential circuits, FPGA AND CPLD Devices.
CEO2: To develop Skills in design of various digital circuits.
CEO3: To work as a group effectively to design and conduct of experiments.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Analyze, measure, interpret and validate the practical observations by applying the conceptual knowledge of digital sub systems.
CO2: Design different combinational and sequential digital circuits at different levels of abstractions for desired specifications.
CO3: Work individually and in groups to solve problems with effective communication.

LIST OF EXERCISES /EXPERIMENTS: (10-12 Exercises/Experiments)

PART- I: (Design and Simulation Experiments)

1. Simulation and Verification of Logic Gates.

2. Design and Simulation of Half adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder and Full Adder.

3. Simulation and Verification of Decoder, MUXs, Encoder using all Modeling Styles.

4. Modeling and Simulation of Flip-Flops with Synchronous and Asynchronous reset.

5. Design and Simulation of Counters- Ring Counter, Johnson Counter, and Up- Down Counter, Ripple Counter.

6. Design and simulation of a N- bit Register of Serial-in Serial-out, Serial in Parallel out, Parallel in Serial out and Parallel in Parallel Out.

7. Design and simulation of Sequence Detector (Finite State Machine- Mealy and Moore Machines)

8. Design and simulation of 4- Bit Multiplier, Divider. (for 4-Bit Operand)

9. Design and simulation of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's COMPLIMENT, Multiplication, Division.

10. Design and simulation of RAM/ROM

11. Mini Projects:
    Form a group of maximum 2 members as a team and assign mini projects related to SoC or NoC based applications.

PART-II: (Implementation Steps for Experiments in Part-I)
1. Verification of the Functionality of the circuit using function Simulators.
2. Timing Simulator for Critical Path time Calculation.
3. Synthesis of Digital Circuit.
4. Place and Router Techniques for FPGA's like Xilinx, Altera, Cypress, etc.,
5. Implementation of Design using FPGA and CPLD Devices.

Total Hours: 14

REQUIRED SOFTWARE TOOLS:

1. Mentor Graphic tools/Cadence tools/ Synopsys's tools.(220 nm Technology and Above)
2. Xilinx ISE 10.1i and above for FPGA/CPLDS.

REFERENCE BOOKS:

1. John F. Wakerly, "*Digital Design: Principles and Practices*", Prentice Hall, 3rd edition, 2000.
2. Digital System Design Lab Manual.

M.Tech. - I Semester
(19MT13832) COMMUNICATIONS AND SIGNAL PROCESSING LAB
(Common to DECS & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

Simulation Lab at UG Level

COURSE DESCRIPTION:

Design and simulation of communication systems - QPSK communication system over AWGN channel and Rayleigh fading channel; Generation of maximal and Gold code sequences; Simulation of Rayleigh Fading Channel Using Either Clarke's Model or Jake's Model for different Doppler Spreads; Performance Evaluation of RAKE Receiver over Slow Fading Channel.

COURSE OBJECTIVES:

CEO1: To design, develop and simulate various components of digital communications and adaptive algorithms.
CEO2: To apply Knowledge and Skills to implement engineering Principles in the fields of Communications and Signal processing.

COURSE OUTCOMES:

On successful completion of this course the students will be able to

CO1: Analyze, measure, interpret and validate the practical observations by applying the conceptual knowledge of communication, signal and Image processing.
CO2: Design IIR and FIR filters for desired specifications.
CO3: Work individually and in groups to solve problems with effective communication.

LIST OF EXERCISES /EXPERIMENTS:

1. Design and Simulation FIR Filter Using any Windowing Technique.
2. Design of IIR Filters from Analog Filters.
3. Generation of Maximal Sequences and Gold Sequences.
4. Performance Evaluation of QPSK System over AWGN Channel.
5. Equalization of Multipath Channel using LMS or RLS Algorithms.
6. Simulation of Rayleigh Fading Channel Using Either Clarke's Model or Jake's Model for different Doppler Spreads (Ex. 50 Hz and 100 Hz).
7. Performance Evaluation of RAKE Receiver over Slow Fading Channel.
8. Performance Evaluation of QPSK System over Rayleigh Fading Channel.
9. Smoothening & Sharpening of a given image.
10. Color image in various color models.

REFERENCE BOOKS/LABORATORY MANUALS:

1. Communications and Signal Processing Lab Manual of the Department.
2. W.H. Tranter, K. Sam Shanmugham, T.S. Rappaport, and K.L. Kosbar, "*Principles of Communication System Simulation with Wireless Applications,"* Pearson, 2004.
3. J.G. Proakis, and M. Salehi, "*Contemporary Communication Systems using MATLAB and Simulink",* Cengage learning, 2nd edition, 2004.
4. R.C. Gonzalez, R. E. Woods, Steven L.Eddins, "*Digital Image Processing using MATLAB", Gatesmark Publishing*, 2nd edition, 2009.

M. Tech. - I Semester
(19MT1AC01) TECHNICAL REPORT WRITING
(Audit Course)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	*2*	-	-	-

PRE-REQUISITES: -

COURSE DESCRIPTION:

Introduction; Process of writing; Style of writing; Referencing; Presentation.

COURSE OBJECTIVES:

CEO1: To impart the knowledge of structure and layout of Business and Technical Reports.
CEO2: To learn styles and techniques of description for effective reports.
CEO3: To develop the ability to understand & interpret the writing techniques for effective communication in written documents.

COURSE OUTCOMES:

After successful completion of this course, the students will be able to:

CO1: Demonstrate knowledge of Technical Report Writing by examining kinds of reports and structure with scientific attitude.
CO2: Apply the techniques in preparing effective reports by examining Techniques of Description, Describing Machines and Mechanisms and Describing Processes.
CO3: Communicate effectively through writing technical reports by demonstrating the knowledge of Industry Reports, Survey Reports, Interpretive Report and Letter Report.

DETAILED SYLLABUS:

Unit I - **Introduction** **(Hours: 06)**
Introduction to Technical Report - Types of Reports - Planning Technical Report Writing - Components of a Technical Report - Report Writing in Science and Technology - Selecting and Preparing a 'Title' - Language Use in Report Writing.

Unit II - **Process of Writing** **(Hours: 05)**
Writing the 'Introduction' - Writing the 'Materials and Methods' - Writing the Findings/Results'- Writing the 'Discussion' - Preparing and using 'Tables'.

Unit III - **Style of Writing** **(Hours: 06)**
Preparing and using Effective 'Graphs' - Citing and Arranging References—I - Citing and Arranging References —II - Writing for Publication in a Scientific Journal.

Unit IV - **Referencing** **(Hours: 09)**
Literature citations - Introductory remarks on literature citations - Reasons for literature citations – Bibliographical data according to ISO - Citations in the text - Copyright and copyright laws - The text of the Technical Report - Using word processing and desktop publishing (DTP) systems - Document or page layout and hints on editing - Typographic details - Cross-references.

Unit IV - **Presentation** **(Hours: 04)**
Giving the presentation - Appropriate pointing - Dealing with intermediate questions - Review and analysis of the presentation - Rhetoric tips from A to Z.

Total Hours: 30

TEXT BOOKS:

1. R C Sharma – Krishna Mohan, *"Business Correspondence and Report Writing,"* Tata McGraw-Hill Publishing Company Limited, New Delhi, Third Edition, 2005 (reprint).
2. Patrick Forsyth*, "How to Write Reports and Proposals",* THE SUNDAY TIMES (Kogan Page), New Delhi, Revised Second Edition, 2010.

REFERENCE BOOKS:

1. John Seely, "*The Oxford Writing & Speaking"*, Oxford University Press, Indian Edition.
2. Anne Eisenberg, *"A Beginner's Guide to Technical Communication"*, McGraw Hill Education (India) Private Limited, New Delhi, 2013.

ADDITIONAL LEARNING RESOURCES

1. http://www.resumania.com/arcindex.html
2. http://www.aresearchguide.com/writing-a-technical-report.html
3. http://www.sussex.ac.uk/ei/internal/forstudents/engineeringdesign/studyguides/tech reportwriting

M.Tech. - II Semester
(19MT23801) ADVANCED WIRELESS COMMUNICATIONS
(Common to DECS & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PREREQUISITES:

A Course on Digital Communications at UG Level.

COURSE DESCRIPTION:

Introduction to cellular wireless communication systems; Radio propagation in mobile environment; Equalization and Diversity techniques; Multiple access techniques; Introduction to wireless networking; Multicarrier modulation techniques.

COURSE OBJECTIVES:

CEO1 : To get introduction of cellular wireless communication and to analyze Radio propagation in mobile atmosphere
CEO2 : To design Equalization along with Diversity techniques and To Solve the problems several access techniques, wireless networking and Multicarrier modulation techniques.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1 : Understand wireless cellular networks and standards, Frequency reuse concept, and solve for Capacity of Cellular Systems.
CO2 : Analyze Large Scale Path Loss, Small Scale Fading in wireless environment, solve engineering problems on power at the receiver in free space propagation.
CO3 : Design and solve engineering problems for analyzing Equalization and Diversity Techniques.
CO4 : Solve engineering problems and calculate with wide range of solutions in Multiple access protocols, Packet Radio and Reservation protocols and Traffic Routing in Wireless Networks,
CO5 : Apply appropriate techniques to engineering activities in MIMO and multicarrier modulation.

DETAILED SYLLABUS

Unit-I: Introduction to Wireless Communication Systems and Cellular Concept (Hours: 09)

Evolution of Mobile Radio Communication Systems, Examples of Wireless Communication Systems, 1G, 2G, 2.5G,3G and 4G Wireless Cellular Networks and Standards, Frequency Reuse Concept, Channel Assignment Strategies, Interference and System Capacity, Trunking and Grade of Service, Improving Coverage and Capacity in Cellular Systems-cell splitting and sectoring. Problem solving.

Unit-II: Mobile Radio Propagation (Hours: 09)

Large Scale Path Loss: Introduction, Free Space Propagation Model, Relating Power to Electric field, Propagation Mechanisms – Reflection, Diffraction, and Scattering. Practical Budget Design using Path Loss Models, Outdoor and Indoor Propagation Models. Problem solving.

Small Scale Fading and Multipath: Small Scale Multipath Propagation, Impulse Response Model of a Multipath Channel, Small Scale Multipath Measurements, Parameters of Mobile Channels, Types of Small Scale Fading (all variations) Statistical Models– Clarke's Model for Flat Fading, and Jake's Model. Problem solving.

Unit-III: Equalization & Diversity Techniques (Hours: 09)

Equalization: Introduction, Survey of Equalization Techniques, Linear and Non-linear Equalizers – Linear Transversal Equalizer, Decision Feedback Equalizer (DFE). Algorithms for Adaptive Equalization – Zero Forcing, LMS, and RLS. Problem solving.

Diversity Techniques: Realization of Independent Fading Paths, Receiver Diversity – System Model, Selection Combining, Threshold Combining, Maximal Ratio Combining, and Equal Gain Combining, Rake receiver. Transmit Diversity–Channel known at Transmitter, Channel unknown at Transmitter – the Alamouti Scheme, analysis.

Unit-IV: Multiple Access Techniques & Networking (Hours: 09)

Introduction to Multiple Access: FDMA, TDMA, CDMA, SDMA, Packet Radio- Pure ALOHA, Slotted ALOHA, CSMA, and Reservation protocols. Capacity of Cellular Systems-Cellular CDMA. Capacity of CDMA with Multiple Cells Problem Solving.

Introduction to Wireless Networking: Introduction to Wireless Networks, Differences between Wireless and Fixed Telephone Networks, Development of Wireless Networks, Traffic Routing in Wireless Networks, Wireless Data Services, Common Channel Signaling.

Unit-V: Multicarrier Modulation (Hours: 09)

Data Transmission using Multiple Carriers, Multicarrier Modulation with Overlapping Sub channels, Discrete Implementation of Multicarrier Modulation –

DFT and its properties, The Cyclic Prefix, Orthogonal Frequency Division Multiplexing (OFDM), Matrix Representation of OFDM, Vector Coding. Challenges in Multicarrier Systems. Problem solving.

MIMO and Multicarrier Modulation: Narrowband MIMO model-parallel decomposition of MIMO channel-MIMO channel capacity-MIMO diversity gain –data transmission using multiple carriers multicarrier modulation with overlapping sub channels-mitigation of subcarrier fading.

Total Hours: 45

TEXT BOOKS:

1. T. S. Rappaport, "*Wireless Communications, Principles and Practice*", Prentice Hall, 2nd edition, 2002.
2. Andrea Goldsmith, "*Wireless Communications*", Cambridge University Press, 2005.

REFERENCE BOOKS:

1. David Tse, Pramod Viswanath, "*Fundamentals of Wireless Communications*", Cambridge University Press, 2006.
2. Dr. KamiloFeher, "*Wireless Digital Communications*", Prentice Hall, 1995.
3. Raj Pandya, "*Mobile and Personal Communication Systems and Services*", Prentice Hall of India, 2002.
4. William C.Y. Lee, "*Wireless and Cellular Telecommunications*", McGraw-Hill, 3rd edition, 2006.

ADDITIONAL LEARNING RESOURCES

1. https://nptel.ac.in/courses/117102062/
2.https://nptel.ac.in/courses/117102062/17
3. https://nptel.ac.in/courses/117102062/17
4.https://nptel.ac.in/courses/117102062/2
5.https://nptel.ac.in/courses/117102062/1

M.Tech. – I/II Semester
(19MT15706) VLSI DESIGN VERIFICATION AND TESTING
(Common to DECS & VLSI)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Courses on VLSI Design, Digital IC Applications at UG Level.

COURSE OBJECTIVES:

CEO1: To impart in-depth knowledge in generation of test vectors for digital systems.

CEO2: To analyze and test the various faults in digital system design and develop fault free applications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Analyze Modeling of Digital Circuits at various levels of abstraction and various types of logic Simulations.
CO2: Understand the various fault models, reduction techniques to apply for fault sampling and simulation.
CO3: Apply the automatic test generation techniques for testing Single Stuck at Faults and bridging faults in digital circuits.
CO4: Analyze the various testing approaches for testing digital circuits with minimal cost.
CO5: Analyze various architectures for Built-In Self Test.

DETAILED SYLLABUS:

Unit –I: Introduction to Testing (Hours: 08)
Modeling-Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Level of Modeling, Logic Simulation- Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

Unit–II: Fault Modeling and Simulation (Hours: 09)
Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, Fault Simulation Techniques, Fault Sampling.

Unit-III: Testing for Stuck Faults (Hours: 09)
ATG for SSFs in Combinational Circuits and Sequential Circuits, Detection of Non feedback and Feedback Bridging Faults.

Unit–IV: Design for Testability (Hours: 09)
Controllability and Observability, Scan-Based Designs and Architecture, Board-Level and System-Level DFT Approaches, Compression Techniques, Syndrome Testing and Signature Analysis.

Unit-V: Built-In Self Test (Hours: 10)
Introduction to BIST Concepts, Test - Pattern Generation, off-line BIST Architectures, Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO.

Total Hours: 45

TEXT BOOK:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, *"Digital Systems Testing and Testable Design",* Wiley, 1st Edition, 1994.

REFERENCE BOOKS:

1. Alfred L. Crouch, "*Design for Test for Digital ICs & Embedded Core Systems",* Prentice Hall PTR, 1st Reprint Edition, 1999.
2. Robert J.Feugate, Jr., Steven M.Mclntyre, "*Introduction to VLSI Testing*", Prentice Hall, 1st Illustrated Edition,1998.

ADDITIONAL LEARNING RESOURCES

http://www2.eng.cam.ac.uk/~dmh/4b7/resource/section16.htm

https://nptel.ac.in/courses/106103016/21

https://nptel.ac.in/courses/106105161/54

M.Tech. - II Semester
(19MT25704) MEMORY TECHNOLOGIES
(Common to DECS & VLSI)
(Program Elective - 3)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Digital Electronics and VLSI design at UG Level

COURSE DESCRIPTION:

Random access memory Technology; Non-Volatile memory designs; Reliability and Radiation effects of semiconductor memory; Packaging technologies, Fault modeling and Testing of memory.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge on various memory Technologies.
CEO2: To develop skills in design and analysis of different memory architectures and Packaging.
CEO3: Apply knowledge and skills to develop optimized memory design to solve real time problems.

COURSE OUTCOMES:

On successful completion of the course, the student will be able to

CO1: Analyze various Random Access Memory Technologies, Non-Volatile Memory Designs and Technologies for optimized memory design
CO2: Analyze the reliability and radiation issues of semiconductor memories for different memory Architectures.
CO3: Analyze advanced memory and high packaging technologies in optimization of memory designs.
CO4: Use the various memory fault models and appropriate testing Techniques to improve the performance of systems.

DETAILED SYLLABUS:

Unit – I: Random Access Memory Technologies (Hours: 11)
Static Random Access Memories (SRAMs): Basic SRAM Architecture and Cell Structures, High performance SRAMs, Advanced SRAM Architectures , BiCMOS SRAMs, Low-Voltage SRAMs ,SOI SRAMs, Specialty SRAMs.
Dynamic Random Access Memories (DRAMs): DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, BiCMOS DRAMs, Cache DRAM, Virtual Channel Memory (VCM) DRAMs, Multilevel Storage DRAMs , SOI DRAMs , Gigabit DRAM Scaling Issues and Architectures, Advanced DRAM design and Architecture, Application Specific DRAMs.

Unit – II: Non-Volatile Memory Designs and Technologies (Hours: 08)
Masked Read-Only Memories (ROMs), Programmable Read-Only Memories (PROMs), Non-volatile memory advances, Floating Gate Cell Theory and Operations, Erasable (UV) - Programmable Road-Only Memories (EPROMs), Electrically Erasable PROMs (EEPROMs), Flash Memories, Multilevel Nonvolatile Memories.

Unit – III: Semiconductor Memory Reliability and Radiation Effects (Hours: 09)
Reliability: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory Reliability, Reliability Modeling, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification.
Radiation: Radiation Effects, Radiation Hardening Techniques- Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics, Radiation hardness assurance.

Unit – IV: Advanced Memory and High-Density Packing Technologies (Hours: 09)
Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto resistive Random Access Memory , Experimental Memory Devices. Hybrids and MCMs (2D), Memory Stacks and MCMs (3D),Memory Cards, High Density Memory Packaging Future Directions.

Unit – V: Memory Fault Modeling and Testing (Hours: 08)
RAM Fault Modeling, Electrical Testing, RAM Peusdo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Application Specific Memory Testing, Memory error detection and correction Techniques.

Total Hours: 45

TEXT BOOKS:
1. Ashok K Sharma, *"Advanced Semiconductor Memories: Architectures, Designs and Applications"*, Wiley Interscience,2003.
2. Ashok K Sharma,"*Semiconductor Memories:Technology*", Testing & Reliability, PHI, 2012.

REFERENCE BOOKS:
1. Kiyoo Itoh, "*VLSI memory chip design*", Springer International Edition, 2001.
2. Luecke Mize Carr, "*Semiconductor Memory design and Application*", Mc-Graw Hill, 1973

ADDITIONAL LEARNING RESOURCES

https://researcher.watson.ibm.com/researcher/view_group.php?id=7956
https://www.electronics-notes.com/articles/electronic_components/semiconductor-ic-memory/memory-types-technologies.php
https://nptel.ac.in/courses/117106111/24
https://nptel.ac.in/courses/106105033/32
https://nptel.ac.in/courses/106104122/30
https://nptel.ac.in/courses/117101058/28

M.Tech. - II Semester
(19MT23802) MIMO SYSTEM
(Common to DECS & CMS)
(Program Elective-3)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Concept of Basic Electronics and Wave Theory at UG level

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in the fields of MIMO.
CEO2: To develop analytical, problem solving, design and application skills in the broad area of MIMO System.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Understand multi-antenna systems, channel modeling and effect of LOS and XPD on MIMO Capacity.
CO2: Analyze diversity and spatial multiplexing in MIMO systems.
CO3: Apply MIMO coding techniques in the field of wireless communication systems.

DETAILED SYLLABUS:

Unit-I: Introduction to MIMO System (Hours: 06)
Introduction to Multi-antenna Systems, Motivation, Types of multi-antenna systems, MIMO vs. multi-antenna systems.

Unit-II: The MIMO Wireless Channel (Hours: 10)
Introduction, preliminaries, MIMO System Model, MIMO System Capacity, Channel Unknown to the Transmitter, Channel known to the Transmitter, Deterministic Channel, Random Channels, Influence of Fading Correlation on MIMO Capacity, Influence of LOS on MIMO Capacity, Influence of XPD on MIMO Capacity, Keyhole Effect: Degenerate Channels, Capacity of Frequency Selective MIMO Channels.

Unit-III: MIMO Diversity and Spatial Multiplexing (Hours: 09)
Sources and types of diversity, analysis under Rayleigh fading, Diversity and channel knowledge. Alamouti space time code, MIMO spatial multiplexing. Space time receivers. ML, ZF, MMSE and Sphere decoding, BLAST receivers and Diversity multiplexing trade-off.

Unit-IV: Space Time Block Codes (Hours: 10)
Space time block codes on real and complex orthogonal designs, Code design criteria for quasistatic channels (Rank, determinant and Euclidean distance), Orthogonal designs, Generalized orthogonal designs, Quasi-orthogonal designs and Performance analysis.

Unit-V: Space Time Trellis Codes (Hours: 10)
Representation of STTC, shift register, generator matrix, state-transition diagram, trellis diagram, Code construction, Delay diversity as a special case of STTC and Performance analysis.

Total Hours: 45

TEXT BOOKS:

T1. Claude Oestges, Bruno Clerckx, "*MIMO Wireless Communications: From Real-world Propagation to Space-time Code Design*", Academic Press, 1st edition, 2010.
T2. Mohinder Janakiraman, "*Space-Time Codes and MIMO Systems*", Artech House Publishers, 1st edition 2004.

REFERENCE BOOKS:

R1. David Tse and Pramod Viswanath, "*Fundamentals of Wireless Communication*", Cambridge University Press, 1st edition, 2005.
R2. Paulraj, R. Nabar and D. Gore, "*Introduction to Space-Time Wireless Communications*", Cambridge University Press, 1st edition, 2003
R3. E.G. Larsson and P. Stoica, "*Space-Time Block Coding for Wireless Communications*", Cambridge University Press 1st edition, 2008.

ADDITIONAL LEARNING RESOURCES

www.sabre.org, www.bookaid.org, NPTEL

M.Tech. - II Semester
(19MT23803) SPEECH PROCESSING
(Common to DECS & CMS)
(Program Elective-3)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Signals & Systems and Digital Signal Processing in UG

COURSE DESCRIPTION:

Acoustic theory of speech production; Models for speech signals and speech processing systems; Mathematical analysis of speech signals - homomorphic and LPC models; Speech and speaker recognition systems.

COURSE OBJECTIVES:

CEO1: To impart knowledge in understanding the concepts of Speech Processing in VLSI.
CEO2: To develop skills in analysis and problem solving using efficient algorithms for feasible and optimal solutions in Speech signal processing field.
CEO3: Apply knowledge and skills for rational analysis of speaker identification and verification systems.

COURSE OUTCOMES:

After completion of the course, the student will be able to

CO1: Understand the process of speech production mechanism and analyze the mathematical model of acoustic speech production system to develop digital model for speech signals.
CO2: Analyze various time domain models such as short time and autocorrelation methods to solve problems in estimating pitch period of speech signals with appropriate techniques.
CO3: Analyze complex Cepstrum of speech, pitch detection and formant estimation in Homomorphic Speech Processing.
CO4: Apply Cholesky Decomposition & Durbin's Recursive approaches to solve LPC Equations in Pitch detection and Formant analysis applications.
CO5: understand speaker verification system, speaker identification systems and Speech recognition systems.

DETAILED SYLLABUS:

Unit-I: Digital Model for the Speech Signal (Hours: 11)
The process of speech production - the mechanism of speech production, acoustic phonetics. The Acoustic theory of speech production- sound propagation, uniform lossless tubes, Effect of losses in the vocal tract, Effect of radiation at the lips, Vocal tract transfer functions for vowels, the effect of nasal coupling, Excitation of sound in the vocal tract. Digital model for speech signals.

Unit-II: Time Domain Models for Speech Processing (Hours: 09)
Introduction, Window considerations, Short time energy and average magnitude, Short time average zero crossing rate, Speech vs silence discrimination using Average energy and zero crossing, Pitch period estimation using parallel processing approach, The short time autocorrelation function, The short time average magnitude difference function, Pitch period estimation using the autocorrelation function.

Unit-III: Homomorphic Speech Processing (Hours: 08)
Homomorphic systems for convolution – properties of the complex Cepstrum, computational considerations. The complex Cepstrum of speech, pitch detection, formant estimation, Homomorphic vocoder.

Unit-IV: Linear Predictive Coding of Speech (Hours: 10)
Basic principles of linear predictive analysis – Auto correlation method, The covariance method. Computation of the gain for the model, solution of LPC Equations – Cholesky Decomposition solution for the covariance method. Durbin's Recursive solution for the autocorrelation equations. Comparison between methods of solutions of LPC analysis equations. Applications of LPC parameters – Pitch detection using LPC parameters, Formant analysis using LPC parameters.

Unit-V: Speech and Speaker Recognition Systems (Hours: 07)
Speaker recognition system-speaker verification system, speaker identification systems. Speech recognition system- isolated digit recognition system, continuous digit recognition system, LPC distance measure.

Total Hours: 45

TEXT BOOKS:

1. L R Rabiner and SW Schafer, "*Digital processing of speech signal*s", Pearson Education, 2006.
2. LR Rabiner, BH Juang, B Yegnanarayana, "*Fundamentals of Speech Recognition*", Pearson Education, 1993.

REFERENCE BOOKS:

1. Thomas F Quateri, "*Discrete time speech signal processing*", Pearson edition, 2006.
2. Ben Gold & Nelson Morgan, "*Speech & audio signal processing*", wiley, 2006.
3. Douglas O Shaughnessy, "*Speech Communications*", Oxford university press, 2nd edition, 2000.

M.Tech. - II Semester
(19MT26305) INTERNET OF THINGS
(Common to CNIS, CS, SE, DECS and CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

Courses on Computer Networks, Python Programming.

COURSE DESCRIPTION:

Concepts of Domain Specific IoTs, M2M and system management with Netconf-Yang, IoT privacy and security, IoT physical devices, Amazon Web Services for IoT and case studies illustrating IoT design.

COURSE OUTCOMES:

CO1: Understand the concepts of IoT, IoT protocols, privacy and security issues in IoT applications to analyze domain specific IoT's.
CO2: Design solutions through implementing IoT applications on raspberry pi, AWS and develop security solutions to strengthen IoT environment.

DETAILED SYLLABUS:

Unit-I: Concepts of IoT (Hours: 07)
Definition and characteristics of IoT, Physical design of IoT – IoT protocols, Logical design of IoT, IoT enabling technologies, IoT levels and deployment templates.

Unit-II: Domain Specific IoTs & IoT and M2M (Hours: 09)
Domain Specific IoTs: Home automation, Cities, Environment, Energy, Logistics, Agriculture, Industry.
IoT and M2M: Introduction, M2M, Difference between IoT and M2M, SDN and NFV for IoT.

Unit-III: IoT System Management with Netconf-Yang and Developing Internet of Things (Hours: 09)
Need for IoT systems management, Simple Network Management Protocol (SNMP), Network operator requirements, NETCONF-YANG, IoT systems management with NETCONF-YANG.
Developing Internet of Things: Introduction, IoT design methodology.

Unit-IV: IoT Privacy, Security and Vulnerabilities Solutions and IoT Physical Devices (Hours: 11)
Introduction, Vulnerabilities, Security requirements and treat analysis, Use cases and misuse cases, IoT security tomography and layered attacker model, Identity management and establishment, Access control and secure message communication, Security models, Profiles and protocols for IoT.
IoT Physical Devices & Endpoints: What is an IoT device, Exemplary device, About the board, Linux on Raspberry Pi, Raspberry Pi interfaces, Programming Raspberry Pi with Python and other IoT devices.

Unit-V: Amazon Web Services for IoT and Case Studies Illustrating IoT Design (Hours: 09)
Amazon Web Services for IoT: Amazon EC2, Amazon AutoScaling, Amazon S3, Amazon RDS, Amazon DynamoDB.
Case Studies Illustrating IoT Design: Home automation, Cities, Environment and Agriculture.

Total Hours: 45

TEXT BOOKS:

1. Arshdeep Bahga, Vijay Madisetti, "*Internet of Things: A Hands-on Approach"*, Universities Press, 2015.
2. Raj Kamal, "*Internet of Things: Architecture and Design Principles*", McGraw Hill, 1st Edition, 2017.

REFERENCE BOOKS:

1. Adrian McEwen, Hakim Cassimally, "*Designing the Internet of Things"*, Wiley, 2013.
2. Jeeva Jose, "*Internet of Things"*, Khanna Publishing, 1st Edition, 2018.

M.Tech. - II Semester
(19MT25702) PHYSICAL DESIGN AUTOMATION
(Common to DECS & VLSI)
(Program Elective-4)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PRE-REQUISITES:

A Course on VLSI Design and Digital IC Design at UG Level.

COURSE DESCRIPTION:

Basics of VLSI design; Layout optimization; Simulation and synthesis; Physical design of FPGAs and MCMs.

COURSE OBJECTIVES:

CEO1: To impart advanced knowledge in Physical Design Automation for Backend Design and Tape out of ICs.
CEO2: To develop and apply skills in design, analysis and solving problems in layouts of Backend Design.

COURSE OUTCOMES:

After successful completion of the course, students will be able to:

CO1: Analyze the various VLSI Design Methodologies and layout compaction in the development of layouts using Design automation tools, FPGA and MCM technologies to implement physical design cycle for the development of reconfigurable designs.

CO2: Apply algorithmic graph theory to reduce complexity in computations using VLSI Design Automation Tools and perform two level and high level logic synthesis to model hardware.

DETAILED SYLLABUS:

Unit – I: Introduction To VLSI Design Methodologies (Hours: 08)
Introduction to VLSI Design automation tools, Introduction to algorithmic graph theory, Computational Complexity, Tractable and Intractable problems, Combinational optimization.

Unit – II: Layout Compaction (Hours: 09)
Design rules, problem formulation, algorithms for constraint graph compaction, placement & partitioning algorithms. Floor planning concepts- shape functions and floor plan sizing, types of routing problems.

Unit - III: Simulation And Synthesis (Hours: 08)
Gate Level Modeling and Simulation, Switch Level Modeling and Simulation.
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

Unit – IV: High Level Synthesis (Hours: 10)
Hardware modeling, internal representation of the input algorithm, allocation, assignment and scheduling algorithms, ASAP scheduling, Mobility based scheduling, list scheduling & force-directed scheduling.

Unit–V: Physical Design Automation of FPGAs and MCMs (Hours: 10)

FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models, MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Routing and Programmable MCMs.

Total Hours: 45

TEXTBOOKS:

1. S.H.Gerez, "*Algorithms for VLSI Design Automation*", John wiley & Sons Pvt. Ltd, 2nd Edition 1999.
2. Naveed Sherwani, "*Algorithms for VLSI Physical Design Automation*", Springer International Edition, 3rd edition, 2005.

REFERENCE BOOKS:

1. Hill & Peterson, "*Computer Aided Logical Design with Emphasis on VLSI*", John Wiley & Sons Pvt. Ltd, 4th edition, 1993.
2. Wayne Wolf, "*Modern VLSI Design Systems on silicon*", Pearson Education Asia, 2nd Edition, 1998.

ADDITIONAL LEARNING RESOURCES

https://nptel.ac.in/courses/106105161/

M.Tech. - II Semester
(19MT23804) SOFTWARE DEFINED RADIO
(Common to DECS & CMS)
(Program Elective-4)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
40	60	100	3	-	-	3

PREREQUISITES:

A Course on Wireless Communication, Digital Signal Processing and Antennas at UG Level.

COURSE DESCRIPTION:

Principles of software defined radio; Multirate digital filter banks; Analysis and Synthesis of signals performance; Smart antennas with applications.

COURSE OBJECTIVES:

CEO1. To provide advanced knowledge in various aspects of Software Defined Radio.
CEO2. To impart analysis, problem solving, design, simulation, Interdisciplinary, Communication and application skills in Software Defined Radio.
CEO3. To imbibe ethical attitude towards environment and society.

COURSE OUTCOMES:

After successful completion of this course the students will be able to

CO1. Understand Radio frequency Implementation issues in software defined radios.
CO2. Design multirate digital filters for multirate signal processing for digital frequency converters in digital receivers.
CO3. Analyze the performance of direct digital synthesis systems in designing software defined radios.
CO4. Apply appropriate techniques for hardware implementation of smart antennas using software radio for better spectrum exploitation.
CO5. Analyze a Software defined Radio System/ Subsystem with object oriented representation for public needs.

DETAILED SYLLABUS:

Unit-I: Introduction to Software Radio Concepts (Hours: 09)
The need for Software radios and its definition, Characteristics and benefits of Software radio, Design principles of a software radio.
Radio Frequency Implementation Issues: Purpose of RF front – end,Dynamic range, RF receiver front – end topologies, Enhanced flexibility of the RF chain with software radios, Importance of the components to overall performance, Transmitter architectures and their issues, Noise and distortion in the RF chain, ADC & DAC distortion, Pre-distortion, Flexible RF systems using micro-electromechanical systems.

Unit-II: Multirate Signal Processing in SDR (Hours: 09)
Sample rate conversion principles, Polyphase filters, Digital filter banks, Timing recovery in digital receivers using multirate digital filters.
Digital Frequency Up-and Down Converters- Introduction- Frequency Converter Fundamentals- Digital NCO- Digital Mixers- Digital Filters- Half band Filters- CIC Filters- Decimation, Interpolation, and Multirate Processing-DUCs - Cascading Digital Converters and Digital Frequency Converters.

Unit-III: Digital Generation of Signals (Hours: 09)

Introduction, Comparison of direct digital synthesis with analog signal synthesis, Approaches to direct digital synthesis, Analysis of spurious signals, Spurious components due to periodic jitter, Band pass signal generation, Performance of direct digital synthesis systems, Hybrid DDS – PLL Systems, Applications of direct digital synthesis, Generation of random sequences, ROM compression techniques.

Unit-IV: Smart Antennas using Software Radio (Hours: 09)

Introduction, Vector channel modeling, Benefits of smart antennas, Structures for beam forming systems, Smart antenna algorithms, Diversity and Space time adaptive signal processing, Algorithms for transmit STAP, Hardware implementation of smart antennas, Array calibration, Digital Hardware Choices-Key hardware elements, DSP processors, FPGAs, Power management issues. Applying Software Radio Principles to Antenna Systems-Smart Antenna Architectures- Optimum Combining/ Adaptive Arrays- DOA Arrays- Beam Forming for CDMA- Downlink Beam Forming.

Unit-V: Object Oriented Representation of Radios and Network (Hours: 09)

Networks, Object –oriented programming, Object brokers, Mobile application environments, Joint Tactical radio system.

Case Studies in Software Radio Design: SPEAKeasy, JTRS, Wireless Information transfer system, SDR-3000 digital transceiver subsystem, Spectrum Ware, Brief introduction to Cognitive Networking.

Total Hours: 45

TEXT BOOKS:

1. Jeffrey Hugh Reed, "*Software Radio: A Modern Approach to Radio Engineering*", Prentice Hall Professional, 2002.
2. Paul Burns, "*Software Defined Radio for 3G*", Artech House, 2002.

REFERENCE BOOKS:

1. Tony J Rouphael, "*RF and DSP for SDR*", Elsevier Newnes Press, 2008.
2. P. Kenington, "*RF and Baseband Techniques for Software Defined Radio*", Artech House, 2005.
3. Paul Burns, "*Software Defined Radio for 3G*", Artech House, 2002.
4. Tony J Rouphael, "*RF and DSP for SDR*", Elsevier Newnes Press, 2008.
5. JoukoVanakka, "*Digital Synthesizers and Transmitter for Software Radio*", Springer, 2005.
6. P Kenington, "*RF and Baseband Techniques for Software Defined Radio*", Artech House, 2005.

M.Tech. - II Semester
(19MT23831) ADVANCED COMMUNICATIONS LAB
(Common to DECS & CMS)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PRE-REQUISITES:

Simulation lab at UG level

COURSE DESCRIPTION:

Simulation of communication systems over communication channels with and without line coding; Design and simulation of Bussgang Blind channel; Minimum Mean Square Error and zero force equalizer; Adaptive equalizers using LMS and RLS algorithms.

COURSE OBJECTIVES:

CEO1: To design, develop and simulate various components of communication System and adaptive equalizers.
CEO2: To apply knowledge and skills in implementation of engineering principles in the field of Communications.

COURSE OUTCOMES:

After successful completion of the course, students will be able to

CO1: Analyze , measure, interpret and validate the practical observations by applying the conceptual knowledge of digital communications and adaptive signal processing.
CO2: Design CDMA communication system over different channels with Various adaptive equalizers for desired specifications.
CO3: Work individually and in groups to solve problems with effective communication.

LIST OF EXERCISES /EXPERIMENTS:

1. Design and simulation of M-ary QAM system with AWGN fading channel.
2. Simulation of Rayleigh fading channel in the mobile environment.
3. Design and performance evaluation of CDMA communication system over a Gaussian channel.
4. Design and performance evaluation of CDMA communication system over a multipath Rayleigh fading channel.
5. Simulation of communication system using convolutional codes & Viterbi Decoding.
6. Design and simulation of an adaptive equalizer using LMS algorithm.
7. Design and simulation of an adaptive equalizer using RLS algorithm.
8. Design and simulation of communication system using Bussgang Blind channel equalizer.
9. BER evaluation for BPSK modulation system with Minimum Mean Square Error (MMSE) equalization in 3 tap ISI channel.
10. BER evaluation for BPSK modulation system with Zero force Equalization in 3 tap ISI channel.

REFERENCE BOOKS/LABORATORY MANUALS:

1. Advanced communication lab manual of the department.
2. W.H. Tranter, K. Sam Shanmugham, T.S. Rappaport, and K.L. Kosbar, "*Principles of Communication System Simulation with Wireless Applications",* Pearson, 2004.
3. J.G. Proakis, and M. Salehi, "*Contemporary Communication Systems using MATLAB",* cengage learning, *2nd Edition,* 2004.

SOFTWARES/TOOLS USED:

MATLAB with communication and Signal Processing tool boxes.

M.Tech. - II Semester
(19MT23832) VLSI DESIGN VERIFICATION AND TESTING LAB

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	4	2

PREREQUISITES:

Course on VLSI Design Verification and Testing.

COURSE DESCRIPTION:

Modeling in HDL, Testing Single and Multiple Stuck at Faults, Testing Bridging Faults, Assessing Controllability and Observability, Test Vector Generation and Compression, BIST.

COURSE OBJECTIVES:

CEO1: To impart knowledge on modeling faults in combinational and sequential circuits.
CEO2: To develop and apply algorithms for testing the digital systems.
CEO3: To develop programming skills to solve problems in assessing fault coverage of developed designs.

COURSE OUTCOMES:

After successful completion of the course, students will be able to

CO1: Demonstrate hands-on experience on modeling faults for digital circuits and estimation of fault coverage and related parameters.
CO2: Develop test generation and test compression algorithms.
CO3: Apply developed algorithms to estimate required parameters for reducing the test time, storage requirements, etc.
CO4: Work individually and in groups to solve problems with effective communication.

LIST OF EXERCISES /EXPERIMENTS: (10-12 Exercises/Experiments)

1. Model a given Boolean Equation or Combinational Logic Design using Hardware Description Language and Assess the Parameters like Area, Delay and Power.

2. Model a given Boolean Equation or Sequential Logic Design using Hardware Description Language and Assess the Parameters like Area, Delay and Power.

3. Model Single Struck at Fault in a given Digital Circuit using Hardware Description Language and Verify it by using
   (i) D – algorithm and
   (ii) PODEM Algorithm

4. Model Multiple Struct at Fault in a given Digital Circuit using Hardware Description Language and develop test vectors that can detect every Single Stuck at Fault but not the Multiple Stuck at Faults.

5. Model Feedback and Non - Feedback Bridging Fault in a given Digital Circuit using Hardware Description Language and develop test vectors that can detect it.

6. Design a Linear Feedback Shift Register and Model it using Hardware Description Language to develop test vectors.

7. Design a Pseudo Random Pattern Generator and Model it using Hardware Description Language to develop test vectors.

8. Model SCOPA Algorithm using Hardware Description Language to obtain Observability and Controllability of each node in the given logic circuit.

9. Model the Partial and Full Scan based Testing using Hardware Description Language and Assess the test methods based on test time, storage, etc.

10. Design a Signature Analysis based on Cyclic Redundancy Checking to generate test vectors by modeling in Hardware Description Language.

11. Develop a Memory Built In Self Test Architecture, model it by using Hardware Description Language and Verify it for various Modes of Operation.

12. Model Compression Techniques based on ones count, transition count, Parity check by using Hardware Description Language and verify its functionality.

13. Mini Projects (MPs):
    Form a group of maximum 2 members as a team and assign mini projects related to Testing of SoC or NoC based applications.

REFERENCE BOOKS/LABORATORY MANUALS:

1. ECE Department Lab Manual on VLSI Design Verification and Testing
2. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Wiley, 1st Edition, 1994.

SOFTWARES/TOOLS USED:

Cadence/ Synopsys/ Mentor Graphics Tools

ADDITIONAL LEARNING RESOURCES

https://www.iitg.ac.in/cseweb/vlab/vlsi/

M. Tech. – II Semester
(19MT2AC01) STATISTICS WITH R
(Audit Course)

(Common to All M. Tech. Programs)

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	-	-	2	-	-	-

PRE-REQUISITES: A course on Statistics.

COURSE DESCRIPTION:
Concepts of R programming basics, Bivariate and multivariate data, Confidence intervals, Goodness of fit, Analysis of variance.

COURSE OUTCOMES:
After successful completion of the course, students will be able to:
CO1: Import, manage, manipulate, and structure data files using R programming.
CO2: Implement models for statistical analysis of a given dataset and visualize the results to identify trends, patterns and outliers in data.

DETAILED SYLLABUS:

UNIT I - INTRODUCTION (Hours : 05)
Data, R's command line, Variables, Functions, The workspace, External packages, Data sets, Data vectors, Functions, Numeric summaries, Categorical data.

Unit II - BIVARIATE AND MULTIVARIATE DATA (Hours : 07)
Lists, Data frames, Paired data, Correlation, Trends, Transformations, Bivariate categorical data, Measures of association, Two-way tables, Marginal distributions, Conditional distributions, Graphical summaries, Multivariate data - Data frames, Applying a function over a collection, Using external data, Lattice graphics, Grouping, Statistical transformations.

UNIT III - POPULATIONS (Hours : 06)
Populations, Discrete random variables, Random values generation, Sampling, Families of distributions, Central limit theorem, Statistical Inference - Significance tests, Estimation, Confidence intervals, Bayesian analysis.

UNIT IV - CONFIDENCE INTERVALS (Hours : 06)
Confidence intervals for a population proportion, *p* - population mean, Other confidence intervals, Confidence intervals for differences, Confidence intervals for the median, Significance test - Significance test for a population proportion, Significance test for the mean (t-tests), Significance tests and confidence intervals, Significance tests for the median.

UNIT V - GOODNESS OF FIT (Hours : 06)
The chi-squared goodness-of-fit test, The multinomial distribution, Pearson's χ^2-statistic, chi-squared test of independence and homogeneity, Goodness-of-fit tests for continuous distributions, ANOVA - One-way ANOVA, Using *lm* for ANOVA.

Total Hours: 30

TEXT BOOKS:

1. John Verzani, *Using R for Introductory Statistics*, CRC Press, 2nd Edition, 2014.
2. Sudha G Purohit, Sharad D Gore, Shailaja R Deshmukh, *Statistics Using R*, Narosa Publishing house, 2nd Edition, 2015.

REFERENCE BOOKS:

1. Francisco Juretig, *R Statistics Cookbook*, Packt Publishing, 1st Edition, 2019.
2. Prabhanjan N. Tattar, Suresh Ramaiah, B. G. Manjunath, *A Course in Statistics with R*, Wiley, 2018.

M. Tech. - III Semester
(19MT33831) INTERNSHIP

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
-	100	100	-	-	-	2

PRE-REQUISITES: --

COURSE DESCRIPTION: Expose students to the industrial environment; Create competent professionals for the industry; sharpen the real time technical / managerial skills required at the job; Gain professional experience and understand engineer's responsibilities and ethics.

COURSE OUTCOMES:

On successful completion of the course, students will be able to

CO1: Develop problem solving skills, critical thinking skills though designing and developing solutions for complex problems.
CO2: Utilize appropriate modern tools and techniques for implementing the proposed solutions.
CO3: Discern various challenges in developing solutions for complex problems, design and conduct experiments to evaluate alternative solutions for the chosen engineering problems.
CO4: Function effectively as an individual and participate well as a team member to build professional network for growth in career.
CO5: Develop communication, enrich professional, interpersonal and technical skills pertaining to the internship experience.
CO6: Utilize real work experiences to explore their interests, career alternatives that will help with future education or employment through and develop professional skills and competencies to engage in lifelong learning.

M. Tech. - III Semester
(19MT33832) PROJECT WORK PHASE-I

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
50	50	100	-	-	20	10

PRE-REQUISITES: --

COURSE DESCRIPTION:

Identification of topic for the project work; Literature survey; Collection of preliminary data; Identification of implementation tools and methodologies; Performing critical study and analysis of the problem identified; submitting a Report.

COURSE OUTCOMES:

On successful completion of the course, the students will be able to

CO1: Apply contextual knowledge to identify specific domain in Digital electronics, Communication systems and allied areas of discipline.
CO2: Conduct literature review, analyze, cognize and comprehend the extracted information to recognize the current status of research pertinent to the chosen domain.
CO3: Select appropriate tools, techniques and resources for implementation of project work.
CO4: Function effectively as an individual to recognize the opportunities in the chosen domain of interest
CO5: Write and present a technical report/document to present the findings on the chosen problem.
CO6: Engage lifelong learning for development of technical competence in the field of Digital electronics and Communication systems.

M. Tech. - IV Semester
(19MT43831) PROJECT WORK PHASE-II

Int. Marks	Ext. Marks	Total Marks	L	T	P	C
150	150	300	-	-	32	16

PRE-REQUISITES: --

COURSE DESCRIPTION:

Time and cost analysis; undertaking practical investigations of project work; implementation; analysis of results; validation and report writing.

COURSE OUTCOMES:

On successful completion of this course, the students will be able to

CO1: Design and develop Integrated Circuits/systems/platforms to undertake practical investigations of project work, analyze and interpret results.
CO2: Utilize appropriate tools, techniques and resources for implementation of project work.
CO3: Function effectively as an individual to recognize the opportunities in the chosen domain of interest
CO4: Write and present a technical report/document to present the findings on the chosen problem.
CO5: Engage lifelong learning for development of technical competence in the field of VLSI.