SREE VIDYANIKETHAN ENGINEERING COLLEGE
(AUTONOMOUS)
Sree Sainath Nagar, Tirupati - 517102

Department of Electronics and Communication Engineering

Three Day Add-On courses
On
'Digital Circuits Modeling by EDA Tools' on 02-04-2019.

EDA tools are most widely used to minimizing time in designing complex ICs, eliminating manufacturing errors, reducing manufacturing costs, optimizing the IC design and simplicity of usage etc. So there is a necessity to learn few tools like Active HDL and Xilinx for the beginners. Here digital circuits are mainly taken for analysis using EDA Tools.

Day 1:

The program started at 08:15 AM on 02/04/19 at ECAD lab by Dr. N. Vithyalakshmi, Associate Professor, Dept. of ECE. Nearly 68 students from II ECE and II EEE passionately attended the program. She keenly explained the importance of EDA Tools, design flow of HDL language, language elements and various levels modeling. She also gave the design idea of circuits used in different kind of research applications using Verilog HDL. Finally the session concluded with student interaction.

Dr. N. Vithyalakshmi, explaining various levels of modeling in verilog HDL

Students who have attended the "digital circuits modeling by EDA Tools"

Day 2:

Hands on session an Active HDL started at 8.15 AM on 03/04/2019 at LDIC lab by Ms.V.Meenakshi, & Mr.Guruprasad, Asst. Professors, Dept. of ECE. They explained basic concepts, complete design flow and execution of the tool. By using Active HDL Tool students actively simulated different digital circuits with various level of modeling and verify the results with the tool.

Ms.V.Meenakshi, explaining the execution of verilog programs in Active HDL Tool

Day 3:

Hands on session on Xilinx ISE 10.1i started at 8.15 AM on 04/04/2019 at ECAD lab by Dr.N.Vithyalakshmi, & Dr.P.Geetha, Asst. Professors, Dept. of ECE. They explained basic concepts, complete design flow and execution of the tool. By using Xilinx ISE 10.1i Tool students actively simulated different digital circuits with various level of modeling and verify the functionality with the tool. Also they analyzed the result with synthesis report and verified the design with RTL schematic, Technology schematic.

Dr. N. Vithyalakshmi, explaining the execution procedure of Xilinx ISE 10.1i

The event had a total of 68 students of II ECE & EEE attended all the sessions of the Add-On Course. The feedback for the event was excellent.