SREE VIDYANIKETHAN ENGINEERING COLLEGE

(Autonomous)

Sree Sainath Nagar, A. Rangampet – 517 102

Department of Electronics and Communication Engineering

Organizes

A Two Day Training Program on "*Mentor Graphics Tools*"

(30th June & 1st July, 2016)

Target Group: **B.Tech (ECE) & M. Tech (VLSI)**

Resource Persons

Mr. Sharath Kumar & Mr. Suneel Kumar,
Application Support Engineer/s
Corel Technologies,
Hyderabad.

Timing: 09.00 AM to 05.00 PM

Venue: Digital IC Design Lab (303)

SREE VIDYANIKETHAN ENGINEERING COLLEGE

SREE VIDYANIKETHAN Engineering College (Autonomous) Accredited by NAAC with 'A' Grade

(AUTONOMOUS)
SREE SAINATH NAGAR, A. RANGAMPET, TIRUPATI

Department of Electronics and Communication Engineering

Report on

A Two Day Training Program on "Mentor Graphics Tools"

Mentor Graphics Corporation is a world leader in Electronic Design Automation (EDA) Tools business.

The IC Nanometer Design bundle provides a complete environment for the design, capture, layout and verification of analog, digital and mixed-signal integrated circuits.

This bundle includes all products that incorporate the IC Nanometer Design platform:

The Pyxis suite of IC design tools

- Schematic capture, netlisting, simulation setup and results viewing.
- Physical layout
- Editing, schematic-driven layout, and top-level floorplanning and routing.

The Questa ADMS analog and mixed signal verification suite

- Questa ADMS and Questa AMDS RF - A language-neutral, mixed-signal simulator that enables top-down design and bottom-up verification of multi-million gate analog/mixed-signal SoC designs.
- Eldo and Eldo RF - An analog simulator offering numerous simulation and modeling options that deliver high-performance and high-speed simulation with the accuracy required by the user.

The Calibre product line for physical verification and design for manufacturability of deep sub-micron integrated circuits

- Calibre - The industry standard platform for physical verification, offering superior performance and capacity for both flat and hierarchical algorithms.
- Calibre xRC - Accurate transistor-level, gate-level and hierarchical parasitic extraction.

Day 1: The program started at 09:00 AM. The concepts of Physical Design Automation were explained by Mr. Suneel Kumar, Corel Technologies, Hyderabad. He explained in detail about the various steps involved in physical design automation. He also addressed about the issues in layout development at submicron region. The program was planned for B.Tech (ECE) and M.Tech (VLSI) students.

The session was later enhanced with introduction to HEP-1 Package and description of Tools. Meanwhile the installation of Tools was done by Mr. Sharath Kumar.

The event had a total of 24 registered participants from M.Tech (VLSI) and B.Tech (ECE). This training program enabled students to perform Physical design Automation of CMOS Designs and Mixed Signal Lab Experiments Easily.

Convener