Report on Guest Lecture, "Analog VLSI Design and its Applications"

The lecture started at 10.00 AM in Dasari Auditorium by Dr. N. Padmaja, Professor, and Department of ECE addressing the participants about the importance of the event. The participants for the expert lecture were 240 Undergraduate students of ECE in SVEC. The Resource person Dr S.Kumaravel, Associate Professor, Department of Micro and Nano Electronics, School of Electronics Engineering, VIT-Vellore.

The resource person took over the session at 10:05 AM discussing overview, Introduction to ICs, recent trends and applications of ICs, Small signal model and design of Analog ICs for future developments. He started the lecture from invention of the ICs, introduced how Moore's law satisfied the present scenario of IC fabrications. He discussed briefly about advancements in microelectronics towards Analog IC design and its modeling. He briefly discussed the different examples for analog integrated circuit designs such as power management circuits, operational amplifiers, and sensors that are used with continuous signals for performing the functions such as active filtering, power distributing for components with in chip, mixing, and so on.

He focused on circuit design and the techniques used to minimize capacitive and inductive noise. He also introduced how to integrate analog circuits on large digital chips presents significant challenges, primarily due to substrate noise coupling. He differentiated a strategy for making analog circuits less sensitive to substrate bounce.

He also summarized that CMOS processes move into the nanoscale—that is, less-than-100-nm—range, it becomes increasingly difficult to maintain the energy efficiency for medium- to high-accuracy analog circuits, Accuracies may decrease as the technology scales down. Analog-chip designers can improve energy efficiency using different approaches, from selecting the optimum CMOS technology to clever system-level design.

Finally he focused on data-converter performance has been steadily increasing over the years. Advancements in scaling and design techniques exploit the high density and speed of modern process technology. More intelligence is being put into data converters. Managing more system functions, converters will simplify programming software, shrink, and become less complex and more cost-effective with digital enhancement. Adaptive power management and sensor integration and enhancement are here, with more to come, eliminating the analog-circuit designer's messy task of signal

conditioning the sensor and keeping the sensor, conditioning, and data-conversion chips as close as possible.

He also discussed ADC converters employing pipeline architecture were the most appropriate for processing wideband signals with the required resolution. He suggested the recent advances in oversampling-data-converter technology have enabled new alternatives for the definition of baseband analog front ends for wireless broadband communication systems. The technology for ADCs using oversampling sigma-delta architectures has evolved to the point that the devices can effectively convert signals with bandwidths of 10 MHz or more. This achievement is significant because it allows for the use of this ADC architecture in the receiver channel of broadband communication interfaces, such as LTE (long-term evolution), WiMax, or 802.11abg.

His current research interest is analog CMOS circuits for transceivers. He also suggested the future scope and research avenues availed in this domain.

The snapshots covering various phases of the event are:

Resource Person Dr. S. Kumaravel being invited to deliver
Guest Lecture by Dr. N. Padmaja, Professor of ECE on behalf of Faculty & Students

Resource person delivering the introductory lecture on evaluation of ICs and its feature sizes.

Participants listening the physics of MOS Transistors

Participants listening general consideration and advancements in CMOS amplifiers.

Participants interacting with the resource person inquiring recent trends and applications in Analog VLSI domain.

Convener