SREE VIDYANIKETHAN ENGINEERING COLLEGE

(Autonomous)

Sree Sainath Nagar, A. Rangampet – 517 102

Department of Electronics and Communication Engineering

Report on

One day Seminar on "**Emerging Trends in VLSI**"

The Seminar started at 9:30AM on 04 January 2013 after conveying the seminar objective and introduction to resource person Dr. N. S. Murthy, Professor of ECE, Dean (Planning & Development) NIT warangal.

85 participants registered for the program and handout materials are supplied to all participants.

During the First Session he delivered lecture on Overview and trends in VLSI design which is focused on VLSI scaling expected to continue for the next decade. The talk was continued on Power Management Issues in VLSI Architectures.

During the Second session he delivered lecture on VLSI DSP architectures with emphasis on DSPP and FPGAs. The talk was continued on ASICs which were customizable architecture to suit for any ideal algorithms. Finally participants interacted with the resource person and cleared their research hurdles in VLSI and Interdisciplinary fields.

Name of the Academic Program : One Day Seminar on **"Emerging Trends in VLSI"**
Duration of the program(Dates**): 04 January 2013**

Outcomes

- Improved Knowledge on emerging trends in VLSI
- Enhanced Research competence in VLSI
- Gained additional knowledge in interdisciplinary challenges related to VLSI.